As semiconductor designs grow more complex, the number of device I/O pins far exceeds the capacity of many testers, and device manufacturers must increase the number and types of test patterns—without increasing test costs. To apply the growing number of scan patterns in a more efficient manner, manufacturers are turning to new test techniques, such as reduced pin-count testing (RPCT). With RPCT, you can apply test patterns using low-cost testers that do not support a large number of I/O pins.

One RPCT implementation relies on the IEEE 1149.1 and 1149.4 boundary-scan Test Access Port (TAP) interface to eliminate the need to connect each device pin to the tester. This approach
facilitates the application of all automatic test program generation (ATPG), BIST, and functional patterns while maintaining compliance to the boundary-scan standards.

Figure 1a depicts a typical boundary-scan implementation that gives full pin access to the tester. In this scenario, the tester drives all primary inputs, including scan input pins, and observes all primary output pins. Typically, the boundary-scan logic is in an inactive state, allowing signals to pass through the boundary-scan cells.

Because of the high cost associated with testers that can support a large number of I/O pins, techniques such as RPCT (Ref. 1) have gained in popularity. By combining RPCT with IEEE 1149.1 and 1149.4 techniques, you can replace high-pin-count testers with lower-cost models for testing digital and mixed-signal devices.

The IEEE test environment

The IEEE 1149.1 standard was originally approved in 1990 to allow board-level access to compliant devices and enable interconnect testing. Since then, this interface has been widely used for chip-level testing as well as for programming onboard devices.

A typical implementation of the IEEE 1149.1 standard uses a boundary-scan cell at each functional pin and configures the cells into a boundary-scan register during test mode. A state machine accessible through a four- or five-pin TAP at the chip’s boundary controls the register. The state machine loads various instructions that enable the user to switch to a standard boundary-scan mode or custom mode. Standard modes such as "Extest," "Bypass," and "Sample/Preload" permit interconnect testing at the board level. Custom modes, enabled by private instructions, give a tester access to internal registers and can be used to initialize and check the status of BIST circuitry.
In boundary-scan compliant circuits, the TCK test clock, which is usually a much slower clock than most of the design’s functional clocks, controls the operation of the TAP controller. Because TCK typically operates at 10 to 25 MHz, the TAP controller cannot easily be used to test most designs at speed.
Reduced pin-count testing

A device configured for RPCT may resemble the circuit shown in Figure 1b, where special RPCT cells that apply and capture values on the primary input and output ports replace the boundary-scan cells on the non-scan ports. The primary input and output pins no longer need to connect to the tester, thus allowing you to use a low-pin-count tester to gain access to scan ports, clocks, and TAP pins.

In this RPCT configuration, the TAP controller remains active during manufacturing test. You would load a separate instruction, corresponding to RPCT, into the TAP controller to configure the boundary-scan cells into a special test mode. This mode must be initialized prior to the application of test patterns and held for the entire set of patterns. The scan and clock pins on a chip use standard boundary-scan cells, such as the BC_1 cell, and in the special test mode function in a pass-through mode where the tester can load serial and parallel data simultaneously. This mode enables the tester to load the boundary-scan register (via TDI/TDO) along with other chains during the scan-shift mode of operation. Assuming that the length of the internal scan chains are longer than the boundary scan register (BSR), the loading of the BSR will not affect the scan load/unload cycle time.

An alternative RPCT setup (Figure 1c) further eliminates the need for tester access to any scan input and output pins. In this approach, concatenating the BSR and the internal scan chains into one long scan chain creates a single scan chain between TDI and TDO. Although it increases test time, this approach allows you to use one of the low-cost boundary-scan testers that are available on the market.

Scan clocking

To employ the TAP controller (as defined in IEEE 1149.1) for testing the internal logic, you must use the TAP controller’s clock (TCK) as the only capture clock for generating test patterns. This use of TCK ensures that the TAP controller reaches predictable and valid states after shift and capture operations. A limitation for using the TAP state machine during ATPG is that TCK can be pulsed once and only once during the capture cycle. This combined with the slow speed of TCK causes at-speed testing to become a distant dream in a standard IEEE 1149.1 environment.

Certain modifications in the BSR and the TAP controller can overcome the limitations of the TAP controller for at-speed testing. During RPCT, you can use your boundary-scan software to place the TAP controller in the "Shift-DR" state and bypass the standard control signals for the boundary-scan cells. This will give the tester full control of the signals needed for shifting data to, and capturing data from, the BSRs. Because the boundary-scan cells appear to be identical to standard ATPG scan cells, you can apply any tests, including at-speed tests, without needing to continuously manipulate the TAP controller.

Mixed-signal RPCT

Designs with mixed digital and analog content introduce other challenges for RPCT. In a purely digital design, every device pin is associated with core I/O and therefore uses a standard boundary-scan cell. The IEEE 1149.1 standard does not provide boundary-scan cells for analog pins; thus, they cannot be controlled during RPCT. This shortfall eliminates the value of RPCT by requiring additional full-pin analog testers to test a mixed-signal device.

Fortunately, the IEEE 1149.4 standard provides special cells called Analog Boundary Modules (ABMs) that interface the digital and analog portions of a mixed-signal device. You can also use an
A typical configuration for a mixed-signal device is shown in Figure 1d. In addition to the RPCT boundary-scan cells, ABMs have been added to the analog input and output ports as well as to the interface between the digital and analog portions of the chip. The use of standard boundary-scan cells on the digital I/O pins of the device allows you to apply parametric test patterns by placing values onto the analog test bus; but be aware that a tester must have full pin access to make the necessary measurements.

**Full chip testing**

![Figure 2. A TAP can provide BIST control of RAM.](image)

You can generally adapt standard IEEE 1149 testing to meet the requirements of most designs. Through the use of BSRs, TAP controllers, and interface pins, you can control and monitor the internal test structures on a device.

For designs that employ BIST technology, you can use an onboard BIST controller to generate and apply test patterns and, in many cases, analyze the results. Because of the narrow pin interface, such designs can be accessed and set up through the standard five-pin TAP interface.

For the memory BIST example in Figure 2, an instruction resets the BIST logic before starting the test. A separate private instruction loaded into the TAP controller initiates BIST in this design. If the tester detects a failure, you can apply memory BIST diagnostics through the TAP controller to capture failure information such as data, address, and the state of the BIST controller.

Typically, the TAP controller schedules multiple BIST controllers to run in parallel or sequentially. Other internal test structures such as logic BIST and special internal scan access can be accessed through the five-pin TAP interface.

For some designs, the length of the longest scan chain may be shorter than the number of I/O pins on the device, which will result in longer scan-chain loading when you use RPCT. To lessen the impact, you can split the boundary-scan register into multiple shorter chains, although this will require additional scan ports to support the new chains. Ultimately, the number of scan channels supported by available testers will limit the number of boundary-scan register segments.

As another option, you can add muxes to bypass the scan and clock ports since these ports are not necessary as part of the shift path. Although this approach complies with IEEE 1149, it adds complexity to the RPCT implementation and may only be appropriate in certain situations.
Experimental results

To determine the impact of RPCT on coverage and pattern count, my co-workers and I configured a small design based on the RPCT methodology. The design had seven internal scan chains where the longest chain had 875 scan cells. The boundary-scan register was 137 cells long and thus did not increase the scan application time. We found that the coverage from the ATPG patterns did not drop significantly, and essentially the same number of patterns were needed for both testing methods (Table 1).

Overall, RPCT provides several advantages and permits the use of low-pin-count, low-cost testers, which helps reduce overall product cost. You don't need to register I/O pins when using BSRs as control and observation points, and RPCT allows board testing from pin to pin using the Extest instruction. The technique also provides a standard access to BIST and other internal test structures, and relies on a simple clocking scheme that allows you to use the system clock and to apply at-speed patterns.

Ultimately, using RPCT does not prevent you from using key test methodologies such as at-speed ATPG, BIST, and functional testing. In fact, using a boundary-scan environment promotes interoperability with other devices on a board and reduces overall test cost.

Table 1. Results of RPCT experiment

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<th>Technique</th>
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