Google power experts share power efficiency techniques at DesignCon 2013

Steve Taranovich - January 02, 2013

DesignCon 2013 will be in Santa Clara, CA this year from January 28-31, 2013.

Created by engineers for engineers, DesignCon enables chip, board and systems designers, software developers and silicon manufacturers to grow their expertise on the latest theoretical design techniques, methodologies and applications, learn about emerging design tools, and network with peers and industry experts.

Conference track highlights include a session on "**Board Power Distribution Techniques Utilizing Higher-than-Traditional Voltages to Exceed Best in Class Efficiency**" by Google power experts Neilus O'Sullivan, Manager Power Group; Uday Ammu, Power Engineer and Mobashar Yazdani, Strategic Silicon Manager.

You will not want to miss this if you are in power management, or even if you just want to bolster your engineering expertise in this area of power efficiency as a non-power engineer.

Power can be distributed on a circuit board at high-voltage but low current, in order to reduce the conduction loss and to minimize the PCB area requirement of the power tracks.

Many techniques exist to help increase power distribution efficiency, but which ones are best suited for your design?

Google power management experts will discuss some proven solutions in this difficult balancing act of trying to provide the optimum power to ensure that processors perform at their best while creating a solid power distribution architecture that will provide efficient use of system power supplies.

Location: Ballroom G

Date: Tuesday, January 29, 2013

Time: 9:20 AM - 10:00 AM

Processor suppliers define power strategies for optimum power-to-performance ratio largely based on 12V architectures, but server efficiency has flattened out at 12V. We have investigated multiple strategies for increasing efficiency, including power regulator architectures as well as higher voltage distribution for servers. Compliance to the strict power management requirements of processors makes it difficult for users to adapt the power network for improvement, including driving it directly at higher voltage.

Google has defined many industry firsts, including using higher voltages for standard processors.

Google's method reduced the multiple power stages that result in mismatched efficiency curves, thereby yielding higher overall efficiency. The session illustrates this efficiency improvement and gives measured results for enabling an ecosystem that pushes the power savings to the next level. Implementing these techniques also affects such aspects as safety; the session also addresses those aspects.