Helping board designers work with high-performance timing

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Being a board designer is a tough job (that’s why this author went into management as soon as the opportunity presented itself). Performing all the necessary tasks to generate the full schematic and guide its implementation requires finding the right trade-offs amongst a plethora of competing needs.

- The Marketing team is demanding a set of features that will barely fit inside the Vehicle Assembly Building at Cape Kennedy, while the Mechanical Design team has allocated a matchbook-sized cubby hole just behind the corporate logo for your board.
- The CTO Office is suggesting some technology they saw in a science-fiction movie last week, while the Purchasing team is insisting you can only use components already on an “Approved Parts List” that is three-quarters vacuum tubes.
- The Software team is refusing to consider a new processor since that might require them to port their code. However their request for 8x the RAM of the last design makes you suspect there’s a performance problem coming your way when this all hits the lab.
- The Power Group has managed to give you an extra 200W of power, but only by giving it to you at 120VAC so that converting it to the needed voltages will count against your thermal budget, not theirs.
- And speaking of thermal budgets, you’ve been asked to make do with 20% less than the last design and the air flow will already be at 75°C by the time it gets to your board.

The last thing you need is to scan the datasheet for the PHY chip you’ve finally got everyone to agree on and see a 3-page table defining its reference clock specifications. A reference clock specification should have frequency and maybe duty cycle. That’s all. It better, because your manager only allowed you 2 days before the final schematic review to get the whole clock tree selected and added.

As most board designers are aware, clock component selection is rarely simple any more. The good news is that the leading companies that design and supply timing components have realized the problems their customers are facing and are providing tools to allow the clock tree to be completed quickly by someone without a PhD in analog design.

Let’s take a look at some of the issues that need to be dealt with when selecting and designing-in clocking components today and discuss the assistance available to get each job done.

Within a board design flow, clocking provides a service function to meet the needs of the architectural building blocks. Until those architectural components are chosen, the full list of clock specifications can’t be determined. Note that some complex communications systems do address some timing functionality, such as network synchronization, in the architectural phase. Once the architectural elements are chosen, their power, area and airflow requirements are taken care of by
the board designer. Then placement-critical components, such as connectors, faceplate switches and LEDs, etc. are added. This often leaves very little board area, power or cost budget for the service components such as glue logic, power supplies and clocking.

**Board Area**

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  In all but the simplest cases, there are multiple clocks needed with different protocols, voltages and performance specifications for each. While each needed function in a clock tree can be simply described and is often available as a discrete component, the cost, area and power penalties of using a separate device for each is not viable. For that reason, timing component suppliers have created components that integrate many functions into a single package. This is intended to assist in achieving an optimal board design, but creates the problem of which set of parts contains the optimal mix of functions for your particular requirements. Also, the trade-off priority between cost, area, power and performance can differ from one design to another.

  Timing component suppliers recognize that their large catalogues of parts represent both an opportunity for an optimal solution and a source of potential confusion. As a result, most timing component suppliers provide either a clock tree builder tool or an expedited service from their knowledgeable Applications Engineers to provide a set of solutions tuned to the requirements of each design. Working with a timing supplier that can offer all the needed components will relieve the digital board designer of the need to fit together several partial and often incompatible solutions.

- **Time-Domain Jitter Limits**

  Time-domain jitter refers to inaccuracies in the placement of the clock edges and can be seen on a regular oscilloscope view of a clock. Cycle-to-cycle jitter represents a very short-term view, one clock edge to the next. It is important in digital logic applications where too short a clock pulse can cause setup or hold time violations. Period jitter is a longer-term view and is important in data recovery applications because excessive period jitter closes the ‘eye’, resulting in a higher rate of bit errors. Both these are dealt with via fairly straight-forward comparisons of the target value versus the timing component’s datasheet. Compliant components can be readily selected through good parametric search tools on a timing supplier’s Web site.

- **Power Consumption**

  Historically, timing components were simple devices with a single power rail and few programmable functions. This allowed their datasheets to contain a single power consumption or current figure and straight-forward comparisons were easy to do. Furthermore, that power consumption number was usually much less than the device’s package could dissipate without airflow or a heat sink, so thermal calculations for that specific chip were not needed.

  Unfortunately, integration and the higher power consumption needed to meet low phase-noise targets, have changed this into a complex and application-specific effort, both from figuring out power consumption and analyzing thermal issues. Many recent timing components offer a high degree of flexibility and the ability to power-down unused functions.
They also offer the ability to power individual circuits at a voltage rail appropriate to the application environment.

Here, the solution is a device configurator tool. Not only will such a tool allow board designers to determine the settings for the timing device, but a properly constructed one will also provide the designer with power consumption and junction temperature estimates that are valid for that particular board and usage.

**Frequency Proliferation**

- Until quite recently, a board designer working in a particular market segment only had to worry about providing 5 or 6 different frequencies, which were fixed once the board powered-up. For example an Ethernet router might need to provide one of 25MHz, 125MHz or 156.25MHz for the line interfaces, depending on which pluggable optics module was installed. Today functionality designed for one market space is rapidly being crossed-over to others. That Ethernet router may now need a USB 3.0 port and an SD-card slot for maintenance, requiring 40MHz and 12MHz clocks. It may also support an Optical Transport Network-compatible uplink port, which could require several of 30-40 different clock frequencies that can change via software configuration. Not only do there end-up being a lot more frequencies, those frequencies are no longer related to one another by simple integer ratios.

These issues are resolved by timing components that offer increased flexibility and multiple PLLs in a single device. However, flexibility tends to add programming complexity. These new components need to come with a configurator tool, such as IDT’s Timing Commander™, that allows a complex device to be setup simply. Just insert the desired input and output frequencies and the tool will figure out how to program all the registers. It will also provide a simple output file for operational software for each frequency plan or to be permanently burned into the part.

- **Frequency-Domain Jitter Specifications**

Frequency-domain jitter refers to unexpected, and usually undesired, extra frequencies that exist in all real-world clock signals. This is most often represented as a plot of the relative energy in a 1 Hz frequency band relative to the energy of the desired frequency (carrier) versus the offset of the frequency from the carrier. These unwanted frequency components are especially bad when present on the reference clock for a high-performance Analog-Digital Converter (ADC) or Digital-Analog Converter (DAC) since those devices will add many aliases of the unwanted frequencies. Also, physical-layer devices (PHY) for high-speed serial interfaces often include ADCs or DACs internally, so frequency-domain jitter is of increasing concern there too.

In high-performance applications, it is necessary to compare the phase noise performance of the timing component to the input specs on the device it drives. Phase noise performance is dependent on the exact configuration of the timing component and so leading configurator tools will show these plots for each setup (see Figure 1).
Signal Protocol and Voltage Shifting plus Power Supply Filtering

The clock tree in a board design is tying together devices from most, if not all, board subsystems as well as frequency sources like crystals and oscillators. As a result there is often a need to convert signals between single-ended (CMOS) protocols and one or more differential protocols (e.g. LVDS) and often to adjust voltage swings as well. This is usually done with networks of passive components, although active level shifters are sometimes used. For a designer not familiar with the current and voltage specifications of each protocol, this used to require wading through a lot of application notes. Configurator tools will provide recommendations on how to deal with these protocol and/or voltage mismatches on either the input or output of a particular timing component (see Figure 2).
The same capability can generate recommended schematics and component values for power supply filters and loop filters that may be required, especially on higher-performance devices.

**Redundancy and Failure Scenarios**

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  As society places increasing reliance on connectivity to carry out our daily lives, reliable operation of everything from mobile handsets through Terabit core routers has become more important than ever. Techniques pioneered for voice telephone switches and fault-tolerant military grade systems have trickled down the network hierarchy. Any system now must be designed in a way to minimize its likelihood of failure (FIT rate) and to minimize the impact if a failure does occur (graceful degradation). Many systems also need to meet international standards such as ITU-T G.8261 for their behavior under failure scenarios.

  For timing components this is mainly about switchover and holdover. Switchover is the process of identifying that one clock source has suffered degradation in quality or total loss of signal and switching to a backup source. Holdover is the end-case of switchover and occurs when all backup clock sources are disqualified and we fall-back on a local crystal or XO to maintain some level of functionality.

  Creating a reliable clock tree is a system-level problem that must be solved at the level of the entire clock tree, especially if an externally-defined, system-level specification must be met. This is a task that still requires a knowledgeable engineer involved. Board designers will need to work with an experienced and system- knowledgeable Applications Engineering team at the timing component supplier to solve these problems today. This is not a problem that can be readily solved on a chip-by-chip basis as those who have tried to mix components from different suppliers can testify.
Summary

Being a board designer is a difficult job requiring ever more in-depth knowledge of a variety of digital, analog, software, thermal and mechanical design topics. In the area of clocking, this has accelerated rapidly in the last 5 years with the proliferation of frequencies, tight time and frequency domain jitter requirements and a mish-mash of different signal protocols and voltage levels. Leading timing component suppliers have recognized this issue and responded with clock tree builder, parametric search and configurator tools with rich yet user-friendly capabilities. These tools provide valuable assistance to the board designer, but can’t relieve the whole burden. For any issues that remain, there needs to be a knowledgeable applications engineering team that understands the system implications of a clock tree. Board designers who work with timing component vendors who provide the tools and application expertise will find their jobs easier and their efforts more successful.