System level design and integration challenges with multiple ADCs on single chip

November 07, 2013

Automotive MCUs catering to markets such as safety, body and chassis and power-train rely highly on sensors and other peripherals on the board for crucial information. They might need to monitor as many as 100 parameters as shown in Figure 1. Since the majority of these sensors and peripherals send out signals that are analog in nature, it is very well implicit that we need to have an analog to digital convertor to sample all these signals and pass them on to the controller so that it can make meaningful decisions.

Now an interesting point emerges, to monitor so many channels one would need multiple ADCs. Another constraint that makes issues more complicated is a limitation on the number of ADC channel pins. We might not have hundreds of ADC input pins ported out. Therefore, to monitor hundreds of signals one might start multiplexing a few of these signals onto a single channel of the ADC. From a systems perspective two more important points are worth noting here. For safety features some of the crucial sensor outputs might need to be monitored with multiple ADCs. Such a feature is necessary to maintain redundancy on certain signals in terms of both measurements and connectivity. Secondly, some customers need to monitor important internal channels to check for the correct operation of the SoC. Some of the Power Management signals and certain supplies etc. are measured through the ADC to diagnose the proper working of the SoC.

Based on what has been discussed we understand that we need multiple ADCs in the system and moreover we would need to multiplex the channels of these ADCs to monitor all of them. Once we understand the need from systems level, let's try to analyze the integration challenges that arise in
order to connect multiple ADCs on a single chip.

Supply and reference

- As we know that ADC has a reference input voltage against which the analog input voltage is compared so if the reference used for conversion is itself not accurate or noisy the overall accuracy of an ADC cannot be guaranteed. The reference noise must not be comparable to 1/2 LSB to avoid loss of bits in output data. Any type of radiated, conducted or electromagnetic emissions can get coupled to the reference or input voltage which degrade the ADC resolution. In multiple ADC architectures we might not have a dedicated set of supply and reference pins for each of the ADC instances as the number of pins available is always a major constraint. So the ADCs might need to share the supply or the reference. This also affects the static and the dynamic characteristic of the ADC in a maximum throughput (minimum sampling and conversion time with ADC clocking at its maximum frequency) mode. Dedicated supplies for each instance may also not be a good idea at times as the different ADCs may show deviation in their results. The power supply should also have a good regulation, which means that when the load is increased from null to full load, the voltage should remain stable over the entire range.

Placement of ADCs in the floor-plan

- ADCs require very careful consideration in the floor plan. I/O pins such as communication protocol pins e.g. I2C, UART, if placed close to the ADC input channels get coupled through the package and a part of the switching current is transmitted to these ADC pins. This is called I/O crosstalk and acts as a source of noise. Shielding the analog signal by placing ground tracks across it helps reduce noise produced by cross talk etc. Noisy systems like SMPS (due to its internal fast switching power transistors) or pins sitting next to the ADC pins might affect ADC’s performance. Constraining such placement options is easy when we have one ADC in the SoC but it becomes extremely tough to manage the padring and SoC floor plan to keep all the ADCs away from noisy systems while maintaining all the below mentioned constraints. The ADC block must be placed close to the input channel pads. It ensures that metal connections can be drawn easily and there is no congestion in the floor-plan. The routing parasitic can be maintained within the defined specs. The input channels, the supply and reference voltages have a shielding requirement as well which complicates routing to a whole new level.

Loading effects on the multiplexed channels

- To understand the loading effect on the multiplexed channel, let’s first discuss the effect of source impedance on the accuracy of the ADC. The analog signal source has some resistance and capacitance that will form an RC network. Now if the charging and discharging of the capacitors could be controlled by \((R_{\text{internal}} + R_{\text{source}})(C_{\text{internal}} + C_{\text{source}})\), then the sampling time of an ADC is increased. The ADC conversion result may not be accurate unless the external capacitor gets charged to the desired analog input voltage level. Now you can see that multiple sensors/channels are multiplexed on the same channel, as shown in Figure 2. So the sampling frequency may even degrade more. The routes to these muxes must be made uniformly so as to maintain the same routing parasitic. It’s very important to maintain uniformity in the routing so that the delay introduced in all the paths is the same. If this is not taken care of then the sampling
time would not be uniform and that would directly affect the throughput of the ADC and its
dynamic characteristics.

![Diagram of complex multiplexing scheme on ADC channels showing external analog muxes and multiple channels connected on the ADC](image)

**Figure 2: Complex multiplexing scheme on ADC channels showing external analog muxes and multiple channels connected on the ADC**

**Characteristics of analog muxes**

- Most of the time our pads are GPIOs which have digital as well as analog functionality. The analog path typically comes from an analog mux placed inside the pad. If the sensor is connected to analog muxes and the output of this connects to the ADC block then the resistance variation inside the analog mux must be taken care of. The resistance of the same analog mux changes with the voltage level applied at its input. Shown in Figure 3. Say an analog mux might show different resistance to a 1.2V input signal vs. a 3.3V signal. This directly impacts the RC parameter of the entire route and thus can impact the sampling time for the same channel which can vary depending on the magnitude of the input voltage.
Once we understand the issues, let us have a look at their resolutions.

- If at all these are cases of shared supply and reference then care must be taken at the package and the die level to maintain as much star-routing as possible so that all loads see equal impedance to the source, and there is little coupling from one load to another that is not common to all loads.

- An ample amount of decoupling capacitors must be placed on such shared supplies to reduce the impact of noise of one ADC on to the performance of the other ADC.

- Effects of analog muxes and channel muxing must be analyzed and simulated well in advance.

- Critical channels should be shielded to avoid signal integrity problems. The shield should be grounded at only one place near the receiver. Grounding the shield at both the ends (source and receiver) may cause ground loops to be formed and making the current flow from the shield.

- Always use different power supplies for analog and digital circuits.

- Use different planes for analog and digital ground to avoid any kind of cross talk. The digital signals usually produce high frequency noise because of fast switching.

- Design should be signed off with DRC, signal integrity, litho and CMP checks.

- If accurate models of noise injection and propagation could be made available, it will help in identifying the PSRR of the circuitry due to noise on supply and reference.

- Sensors that directly give a digital output can be used, thus the need for more and more analog channels can be reduced.
√ Make sure that top-level optimization, buffer insertion, signal-integrity improvements and DRC fixes do not negatively impact sensitive analog routes and analog/digital interfaces

More about the authors

Kushal Kamal
Vandana Sapra