Guard techniques for high-Z test-point muxes

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A multiplexer (or mux) is a device that selects one of several input signals and forwards the selected input into a single line. It is widely used in automated testing platforms, because it saves both test time by eliminating manual connections, and cost by using one measuring unit [1]. One common way to implement a mux is to use reed relays [2]. A reed relay often has a small size, and its on-resistance is usually smaller than solid-state counterparts. Those features make reed relays a popular choice in matrix and multiplexer modules [2] [3].

But large muxes can put undue capacitive loading on a test point, leading to frequency limitations and/or instability. This article describes a mitigating approach.

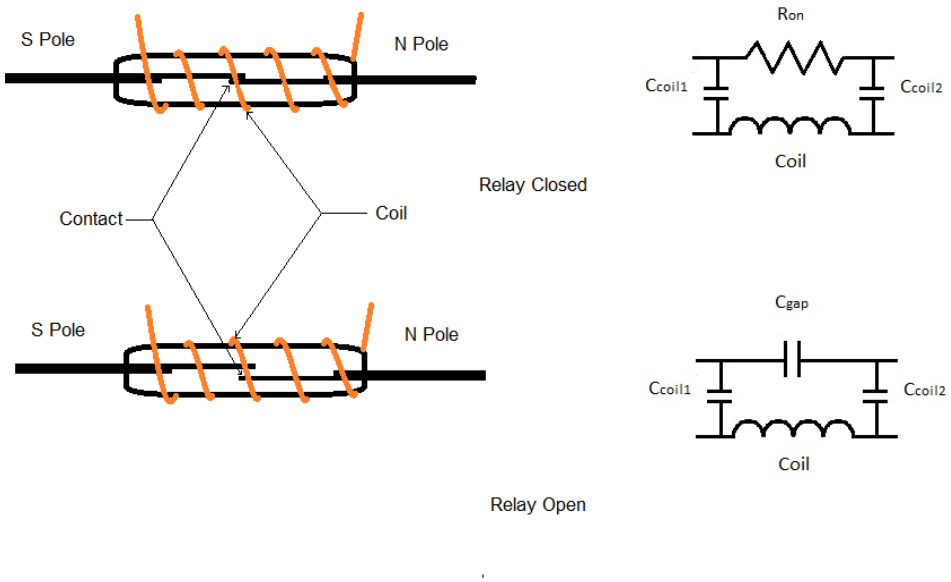

Figure 1 Reed relay closed (top), and open (bottom), and their parasitics

Figure 1 illustrates the structure of a reed relay, and its equivalent circuit models [3]. The non-ideality of a reed relay mostly comes from its on-resistance (R_{on}), capacitance between open contacts (C_{gap}), and capacitance between contacts and coil ($C_{coil1,\,2}$). Nevertheless, those non-idealities are negligible in most moderate-frequency applications. The example below explains why:

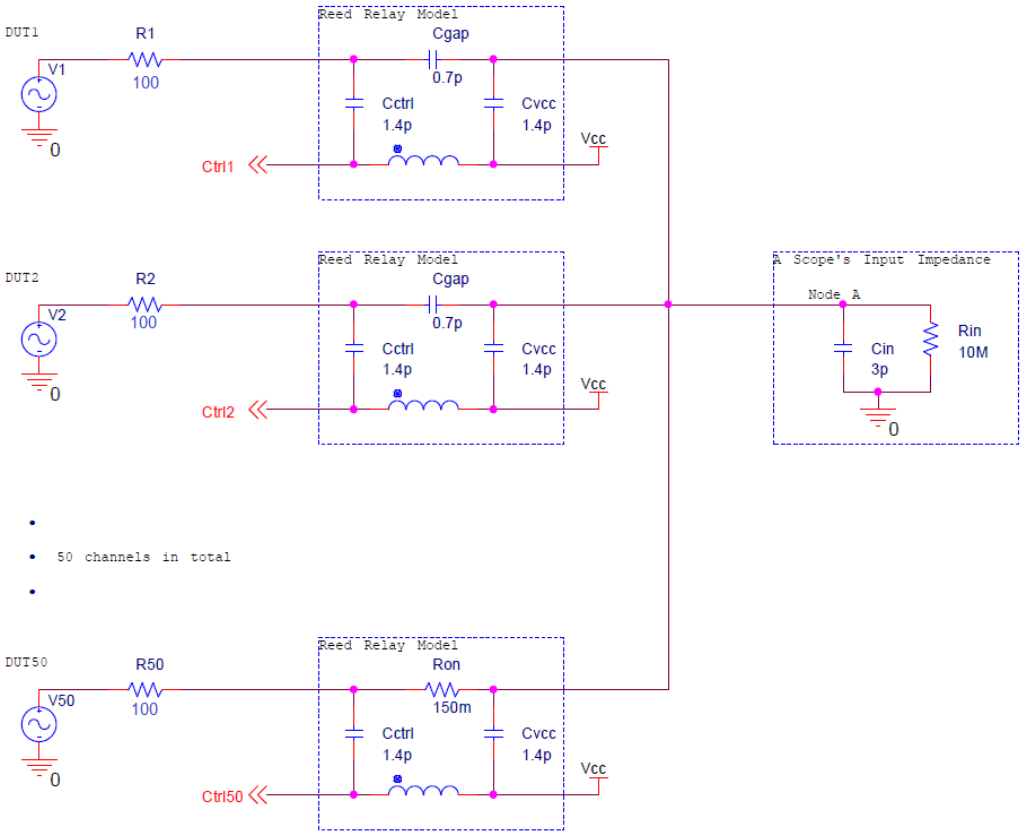

Figure 2 50-channel mux with one reed relay on each channel

Figure 2 illustrates a typical application when a reed relay mux is used. The values of parasitic components in the reed relay model are based on Coto Technology's 9000 series reed relay [4]. Those values are typical for a reed relay. V_{CC} is the coil biasing voltage. Ctrl n (n = 1, 2, …, 50) goes to relay drivers. C_{Vcc} and C_{ctrl} are the equivalent capacitors between one of the relay contacts and coils. The voltage sources with 100Ω output resistors represent DUTs. C_{in} and R_{in} (3pF, 10MΩ) model the input impedance of a scope, a typical measuring instrument. There are 50 channels. Channel 50 is connected to the scope, while all the other channels are open. The disconnected voltage sources (DUT1-49) are off.

Let's determine the mux's bandwidth. The input of the scope, node A, is the node that has the highest capacitance in this network, and there is at least 50 × 1.4 pF C_{Vcc} in parallel. Therefore, the 100Ω in series with open relays is negligible compared with the impedance of C_{gap} at the frequency that impedance at node A is comparable to 100Ω. C_{ctrl50} can be considered as open circuit for the same reason. The coils have a DCR much higher than 100Ω [4]. We therefore consider that as open circuit, too. We therefore can simplify the network to the one in Figure 3.

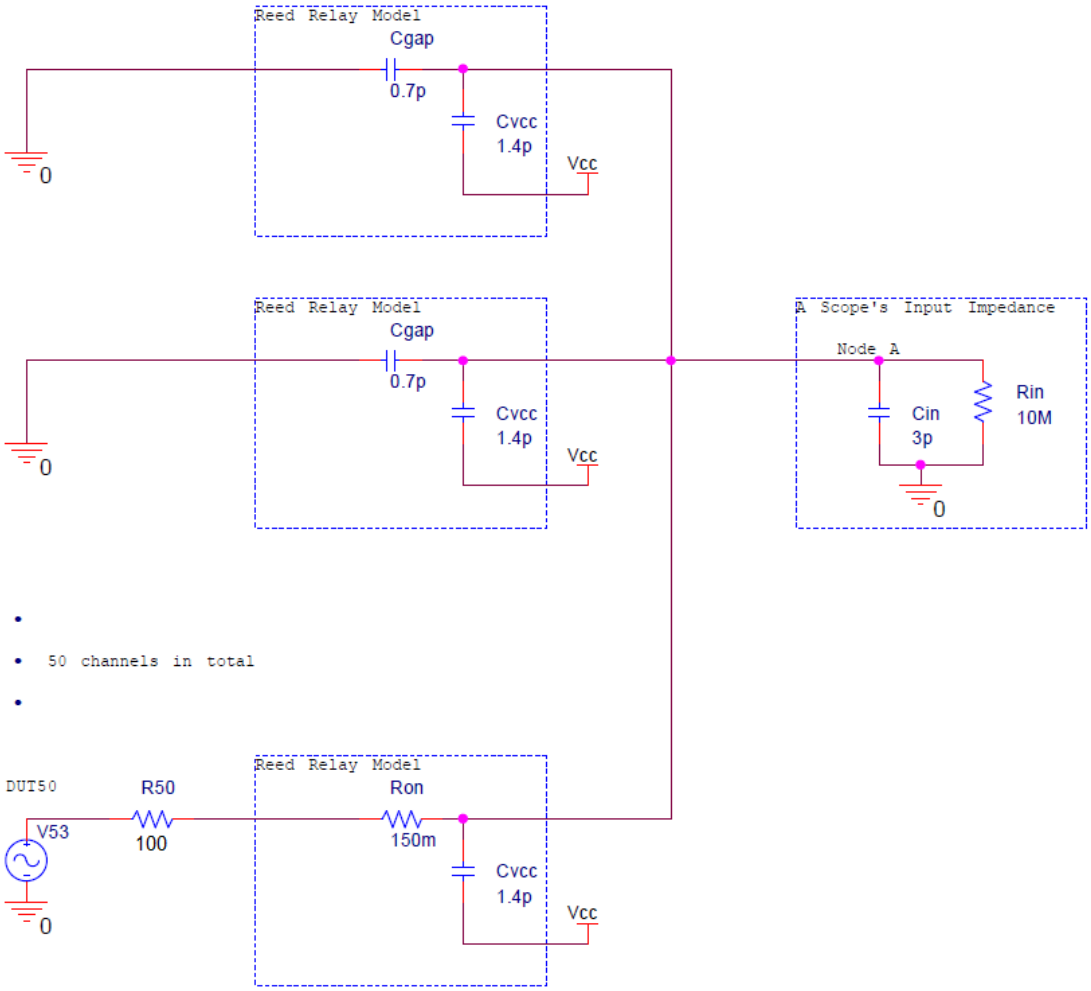

Figure 3 Simplified network for -3dB frequency calculation

The -3dB frequency of this network is:

$$f = \frac{1}{2\pi(R_{50} + R_{on})[C_{vcc} + 49(C_{vcc} + C_{gap})]} = 13.3MHz$$

That is to say, for moderate frequency applications up to a few megahertz, the reed relay mux functions almost as ideal wires.

High-Z test-point applications

However, this will not be the case if the DUT's output has high impedance.

Consider the network in Figure 4, and the equivalent circuit model in Figure 5. This is similar to Figure 3 except the DUTs are now current sources. SPDT relays are used here because the current sources can't be left open. R_{load} translates current signals to voltage to be measured by the scope. With R_{load} of 20kΩ, the -3dB frequency is only 60kHz, assuming the relays' parasitic capacitances remain similar. In real life, because of extra capacitance introduced by the PCB and cables, this number will be even lower. This makes the mux not very useful at frequencies beyond a few kilohertz.

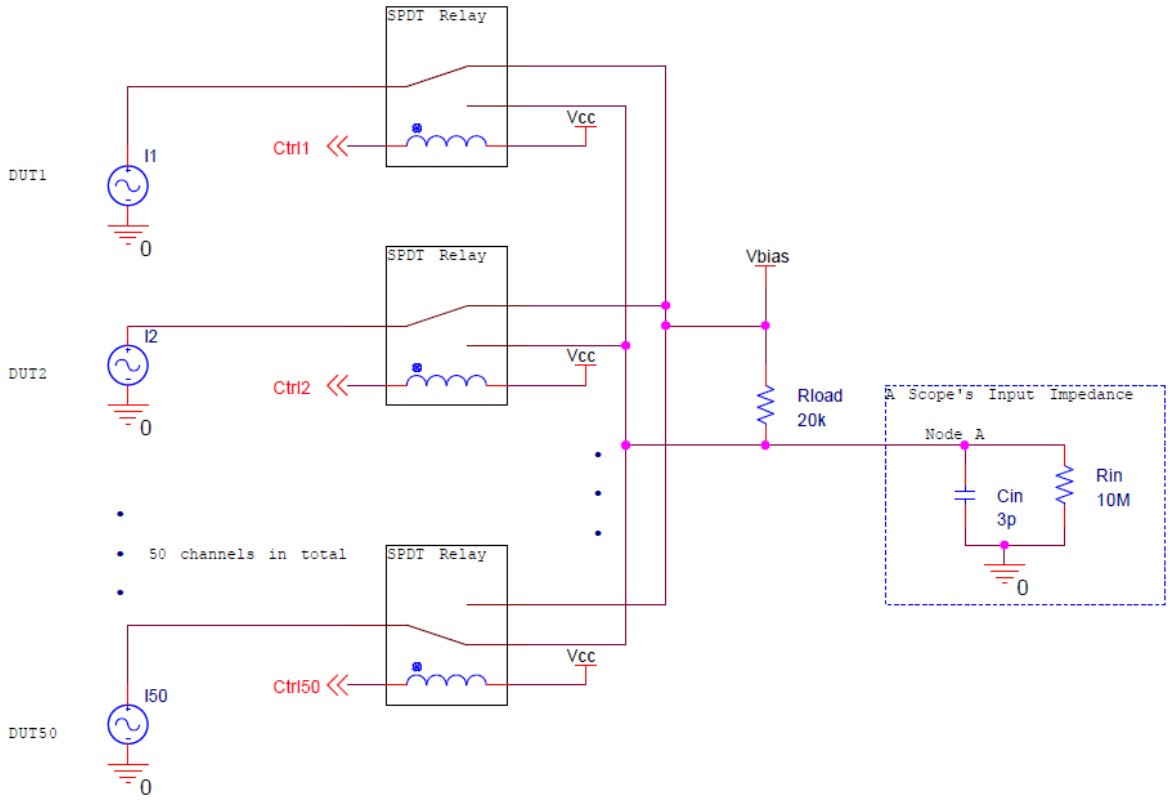

Figure 4 50-channel mux for current source DUTs

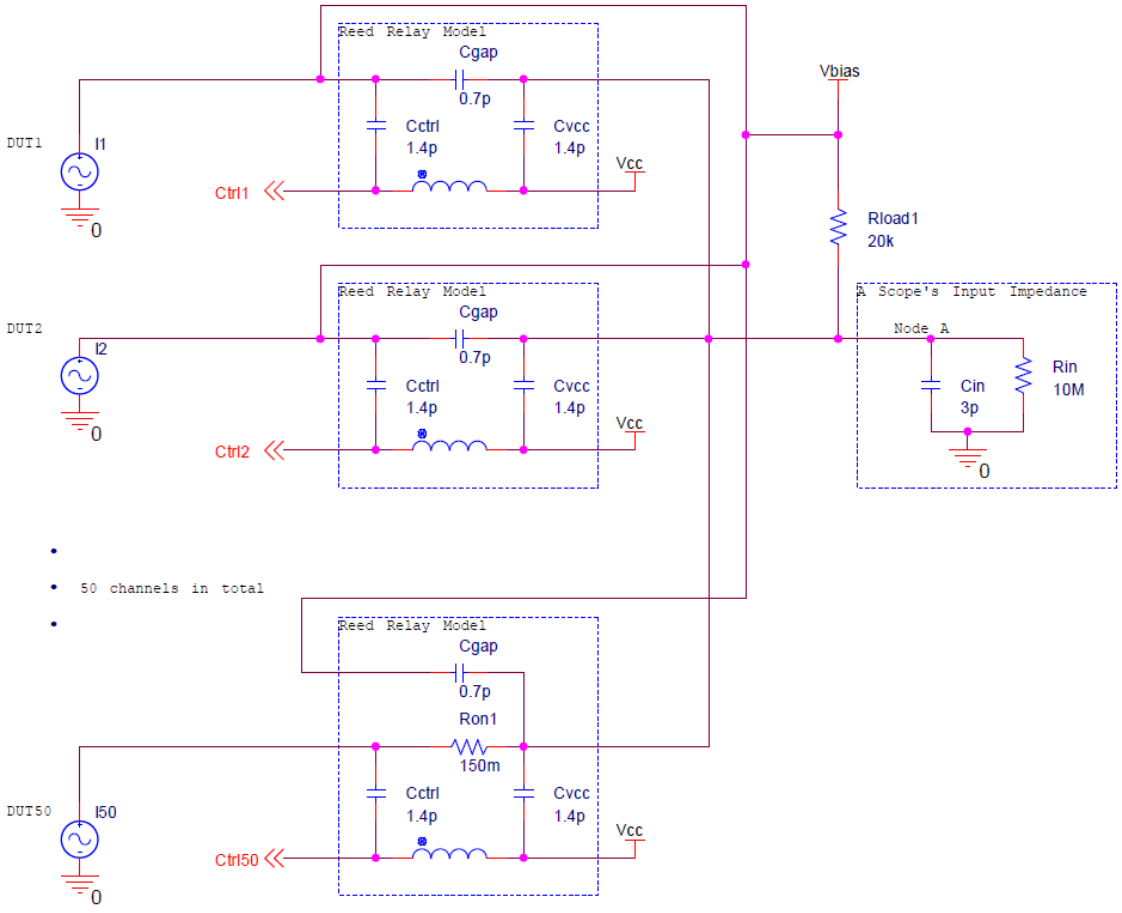

Figure 5 50-channel mux circuit model

This scenario can arise when the DUT is a current source with a high impedance load, or a voltage source with high output impedance (a current source is used in the examples below).

We will introduce techniques that reduce capacitance at the node A common. This can extend the bandwidth of the mux, making it useful even for high-Z applications. It worth pointing out that reducing the capacitance not only benefits bandwidth, but also helps stability for some lower impedance applications where the output is tied to feedback such as an op-amp. It can also aid tests with high slew rate, such as amplifier or LDO step response.

Guard techniques

To approach this problem, we first identify two major capacitive current paths in Figure 5. They are marked in red in Figures 6 and 7. Obviously, the key to solve the problem will be to find ways to eliminate or reduce the capacitive current in those two paths.

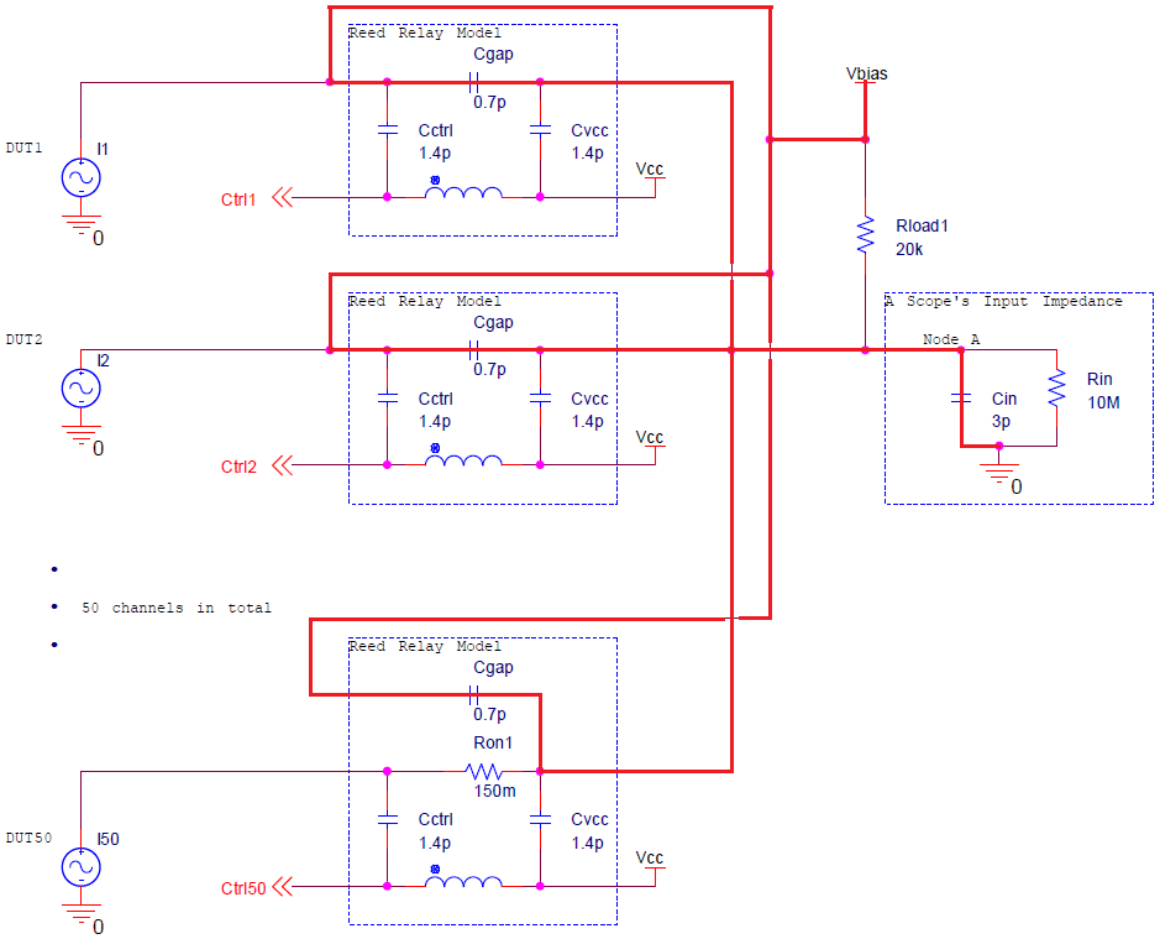

Figure 6 Capacitive current path #1

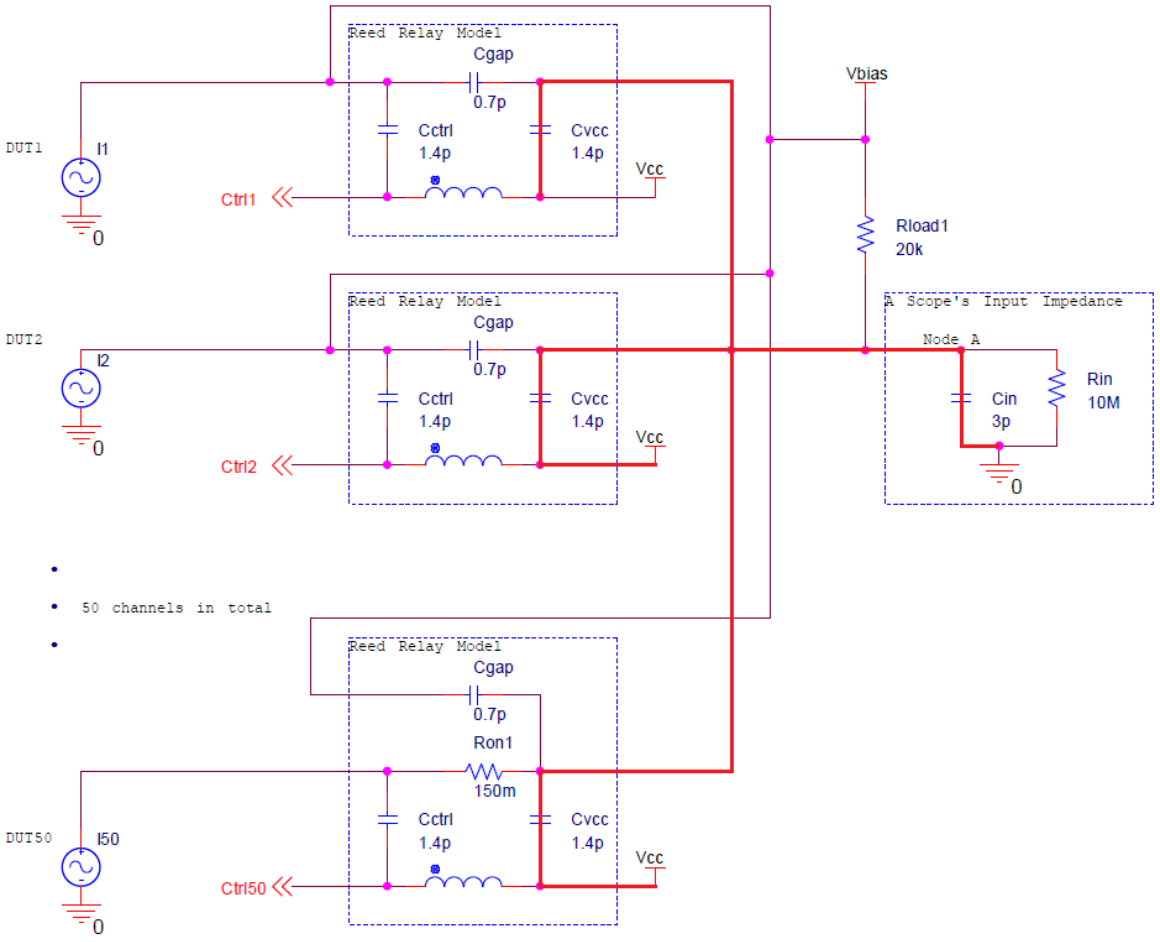

Figure 7 Capacitive current path #2

Cancelling C_{gap}

First, let's take a look at the path in Figure 6. This path passes through 50 × C_{gap} of the open relays, and ends at a DC bias source, V_{bias}.

You may ask: what if we keep the current sources off when not under measurement, and don't connect them to any voltage sources? (i.e., use SPST relays) Won't this solve the C_{gap} issue? The answer is most likely, no.

First, even if the current sources are off, they will have output capacitance in parallel with them. That can shunt C_{gap} to ground if large.

Second, even if the output capacitance is so small that is negligible, C_{gap} will still connect to C_{ctrl}, which goes to a relay driver, including a catch diode in parallel. Their output capacitors will then connect C_{ctrl} to ground. Those capacitors are typically comparable to C_{ctrl}, if not much larger. Therefore, the total capacitance at node A will still be large, because of the number of channels. Therefore, we will keep the SPDT relay configuration. In fact, this configuration will help us cancel C_{gap}.

How do we cancel C_{gap}? Capacitor current is formed when the capacitor voltage changes:

$$I = C\frac{dU}{dt}$$

Since the voltage at node A varies, can we make the voltage across C_{gap} constant by varying the other side of C_{gap} the same way? Yes. This is how the SPDT configuration becomes helpful. It connects the other side of each C_{gap} together, making this node easy to access. We can use a DC + AC source whose AC component is exactly the same as at node A. Figure 8 shows one way to do it:

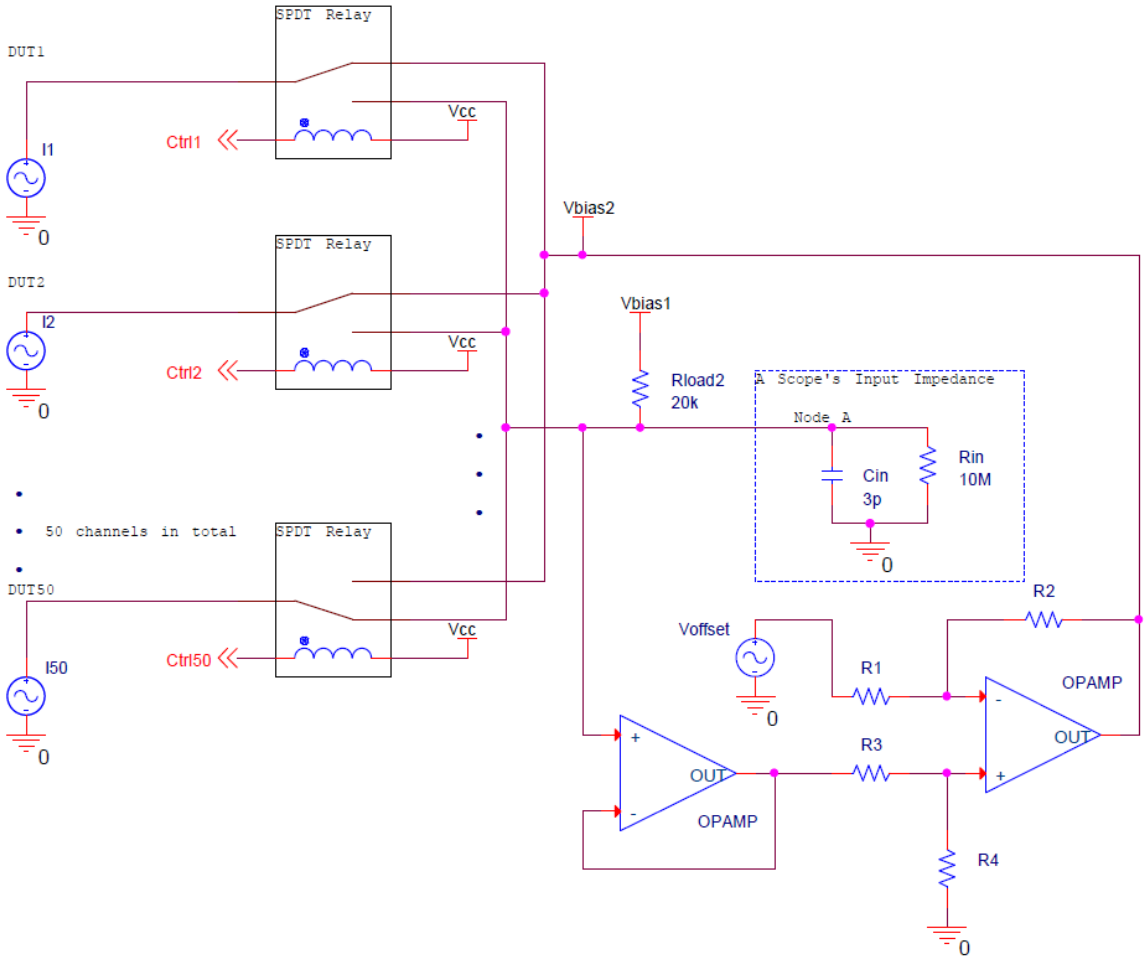

Figure 8 Cancelling C_{gap}

In Figure 8, the signal at node A is buffered. R1-R4 are the same value. The output of the diff-amp is:

$$V_{bias2} = V_A - V_{offset}$$

V_{offset} is a DC offset voltage that can go both positive and negative. It is used to set the proper DC bias value for the current sources not being measured.

The method in Figure 8 needs two op-amps, unless V_{offest} is zero. In that case, the buffer's output can connect to V_{bias2} directly. We can save one op-amp if a floating DC power supply is available. Figure 9 shows a circuit achieving the same result, using a floating DC source.

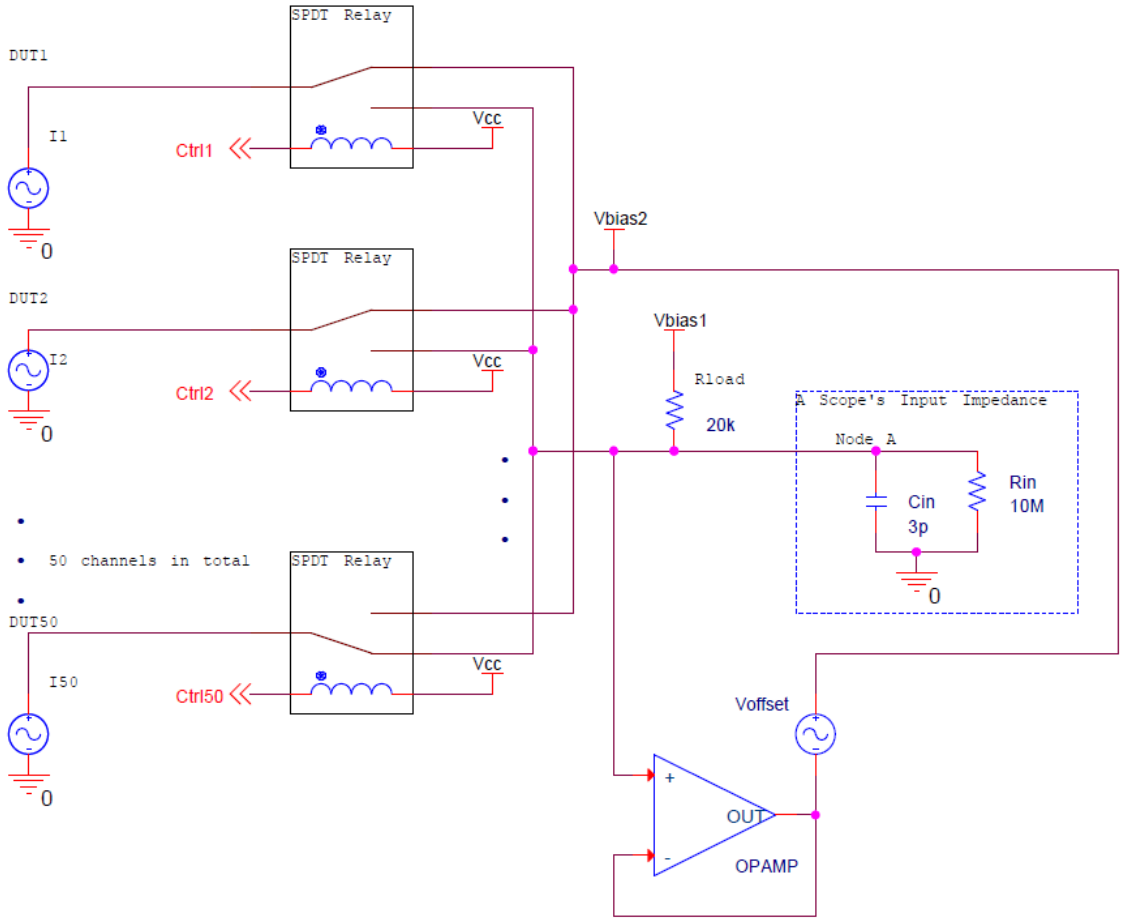

Figure 9 Cancelling C_{gap} using a floating DC source

Fortunately, many benchtop power supplies' output stages are isolated by transformers and are essentially floating (e.g., Keysight E3631A, E3646A). The capacitance between the negative terminal and ground is negligible in this application.

Figure 9's circuit is simpler than Figure 8, but still needs an active component, which complicates the setup. Figure 10 shows a circuit which will work in a special though not uncommon case, using only a resistor:

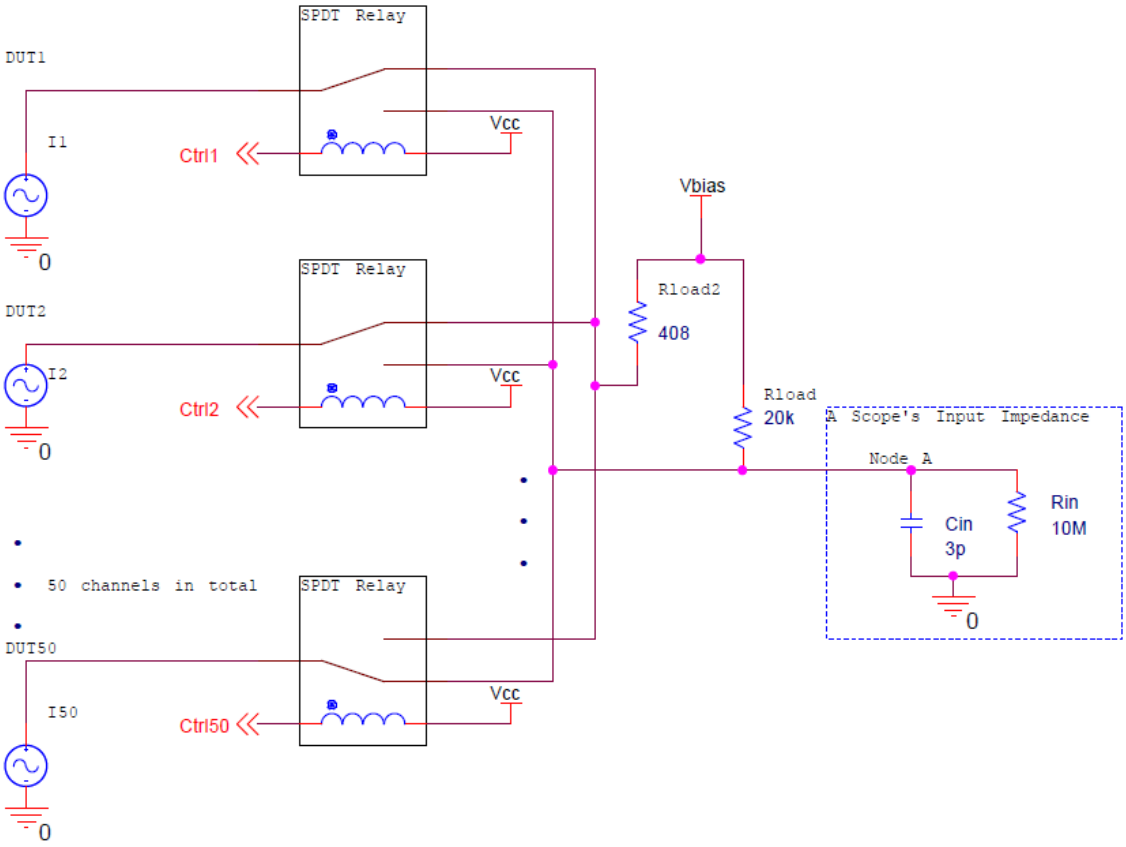

Figure 10 Cancelling C_{gap} using another load resistor

If DUTs on different branches of the mux are identical, and the application allows the DUTs to remain on when not being measured, then we can have all DUTs output the same current waveform as the one under measurement. R_{load2} is selected as:

$$R_{load2} = \frac{1}{n-1} R_{load}$$

Where n is the total number of DUTs, which in this case is 50.

$$V_{node\ A} = I_{50} R_{load} = (n-1) I \frac{1}{n-1} R_{load} = \sum_{n=0}^{49} I_n R_{load2}$$

Where I is a single DUT's current. $I_n = I$. $n = 1,2,\ldots 50$.

Using the cancelation techniques above, the voltage across C_{gap} will stay the same. No current will flow through C_{gap}, and it will no longer load node A.

Cancelling C_{Vcc}

After the current path through C_{gap} is taken care of, we turn our attention back to the path in Figure 7. This path is formed mainly by C_{Vcc}. The loading current eventually flows to V_{CC}, the DC voltage that biases the relays' coils. Given our previous experience, we naturally come up with Figure 11: driving V_{CC} with an AC component the same as node A. Here we use floating voltage sources just to illustrate the concept.

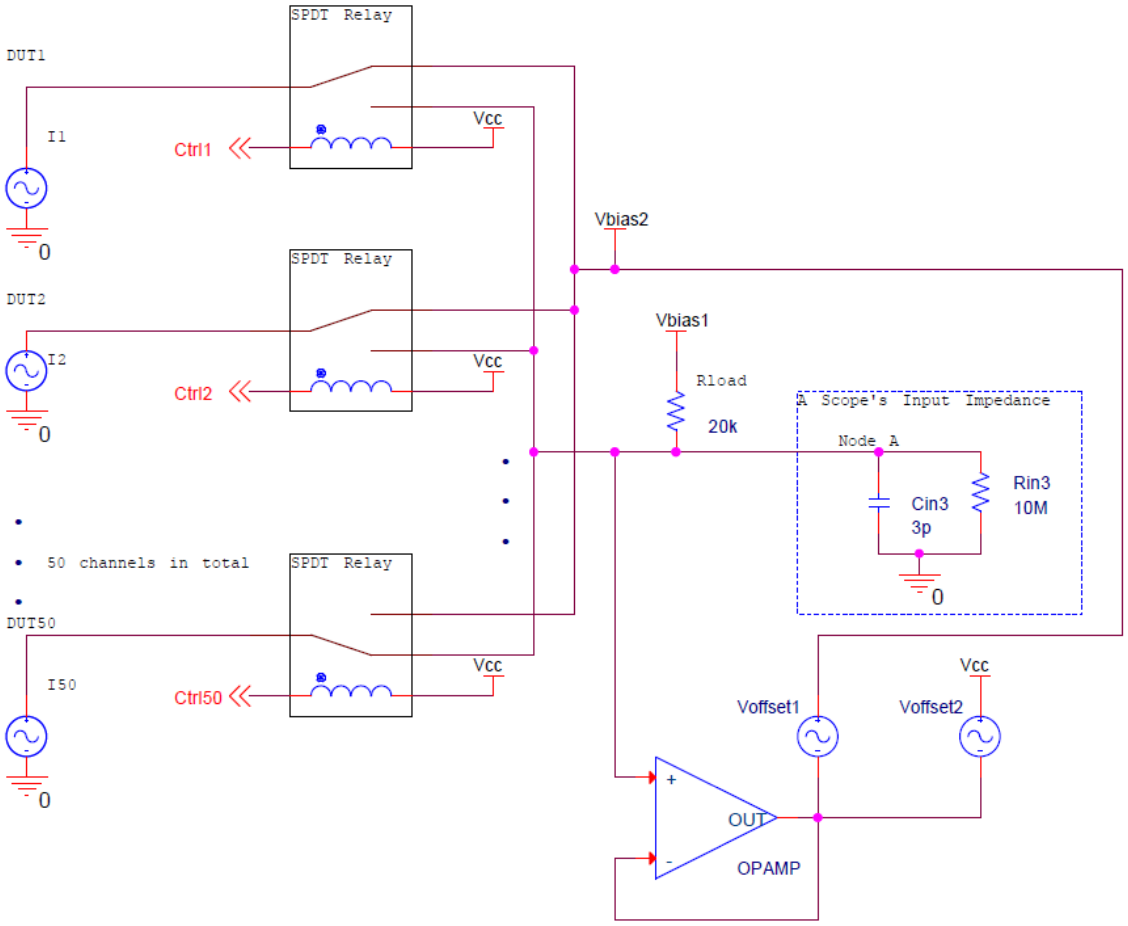

Figure 11 Driving V_{CC} with an AC + DC source

It looks like this circuit should have the parasitic capacitors at node A taken care of. However, experiment showed it was not the case, though there was improvement. Why? We need to take a closer look at the coil model.

The coil is not a wire even at DC. It has a resistance of about 100Ω. As we have pointed out, a relay driver has a relative large output capacitance. For simplicity, we consider an extreme case: relay driver's output capacitance is so large that one end of the coil can be considered shorted to ground. The capacitance between a relay's pole and its coil is actually distributed along it length, illustrated in Figure 12. That means driving the coil-bias voltage won't eliminate all the parasitic capacitance between the coil and pole.

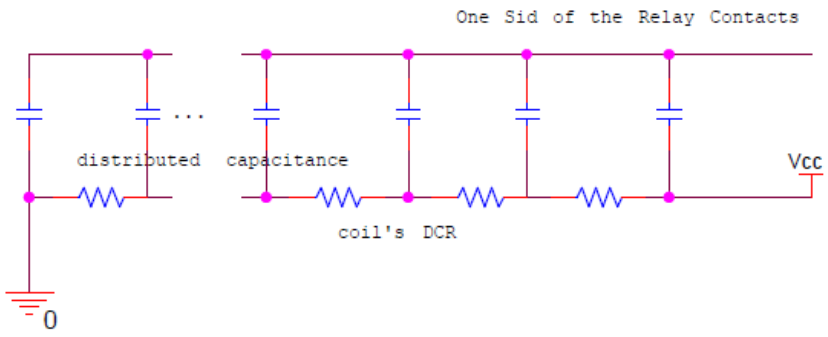

Figure 12 Capacitance between pole and coil

Knowing where the issue comes from, we arrive at the circuit in Figure 13 (catch diodes are not shown for simplicity). Here the V_{SS} of the relay drivers is driven by the AC component of node A with 0 V offset. As a result, both ends of the relay coils are driven by the same AC component: the parasitic capacitors between coil and relay contacts are virtually gone.

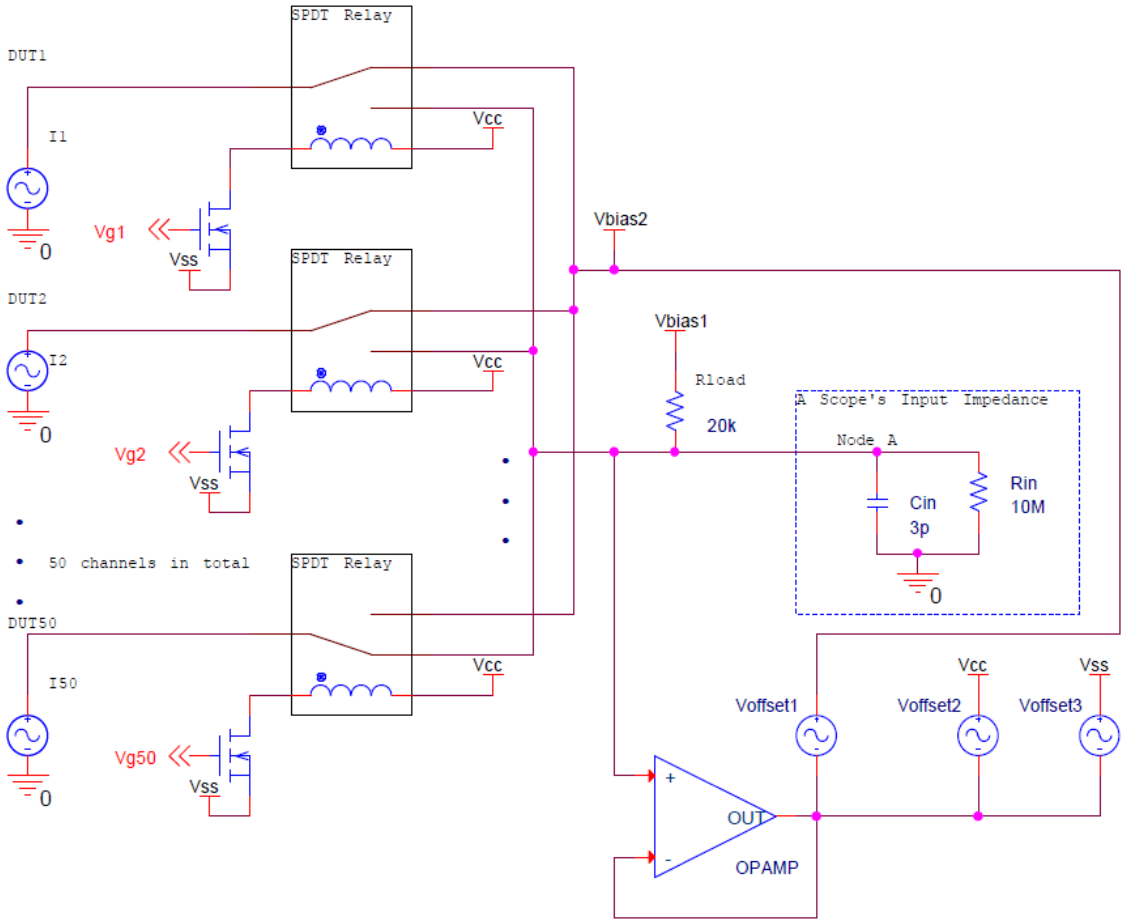

Figure 13 Driving both V_{CC} and relay driver's source with an AC + DC source

Since the FET source of the relay drivers is not ground any more, will the relay driver operate properly all the time? The circuit in Figure 13 can only work if a relay driver's gate voltage minus the AC amplitude at V_{SS} is larger than relay driver's turn on voltage. If the AC amplitude gets larger,

we will have to increase the relay drivers' gate voltages accordingly.

Other concerns

So far, we have explored techniques to cancel a reed-relay mux's parasitic capacitors for current source applications assuming ideal circuits. However, components in real life are not ideal. Therefore, we need to follow good engineering practices to minimize impact from non-idealities:

Relay selection

It is better to choose relays of smaller parasitic capacitance to start with. Most of the parasitic capacitance will load the op-amps. A smaller load introduces less phase shift and attenuation, so the parasitics will be better canceled if they are smaller.

In Figure 10, even with R_{load2}, equivalently speaking, each current source still needs to drive one C_{gap}. Therefore, it helps if C_{gap} is small from the start.

Shielded relays

An electrostatic shield (Figure 14) is a layer between a coil and contacts designed mainly for noise immunity (do not confuse with a magnetic shield). In most applications, it is grounded or connects to a DC source. A shield reduces both the capacitance between contacts, and between contacts and coil, but introduces extra capacitance between contacts and shield.

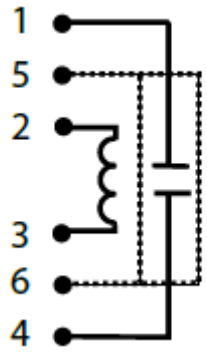

Figure 14 Relay with electrostatic shield [4]

If a shield exists, drive it the same way you drive coil V_{CC}.

Layout considerations

Standard FR4 PCB materials have a dielectric constant from 4.1 to 4.4. If there are two layers of 30mm by 30mm copper 10mils (0.254mm) apart, the cap in between will be:

$$C = K \times E_o \times \frac{A}{D} = 135pf$$

Where $E_O = 8.85 \times 10^{-12}$, K = 4.3, A is the area, and D is the distance.

On a board that holds 50 reed relays, the traces connecting all the relays' pins, both coil pins and contacts, will comprise a significant area. It is thus critical to avoid copper pour close to those traces.

Because of this, the noise immunity of this PCB may not be great. If it is a noise-sensitive application, you can surround the board with a shielding enclosure.

When connecting an op-amp's output to the pins of relays, the layout pattern is significant. A fan-out style means longer total trace length, and therefore, larger trace capacitance. But the advantage is the capacitance of the traces to each relay will be similar: the capacitance canceling circuit will deliver similar performance on each channel.

A daisy-chain style, on the other hand, yields smaller total capacitance at the output of the op-amp at the price of inconsistent performance on different channels.

We therefore recommend a combination of both styles so that we can trade off the features above. Figure 15 shows the style.

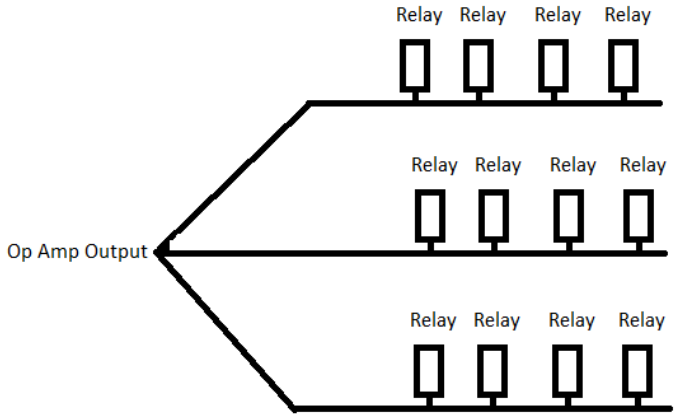

Figure 15 Segmented daisy-chain layout style

Experiment

A mux was built to test one of Broadcom's multi-channel current source IPs using the circuit in Figure 16. The DC components of the current sources were zero. A triple-output power supply (Keysight E3631A) was used to provide dual op-amp supplies and the floating voltage.

Before these techniques were applied, the capacitance at node A was about 300 pF. With an improved layout, it decreased to about 200 pF. By adding R_{load2}, the equivalent capacitance was reduced to about 150 pF. Driving coil bias voltage V_{CC} with an AC + DC voltage, the capacitance was further reduced to about 30 pF. With V_{SS} driven too, less than 10 pF was left. The remaining capacitance at node A was most likely from cables, connectors, and layout of components other than the relays. The -3dB frequency of this mux was extended by more than 30 times.

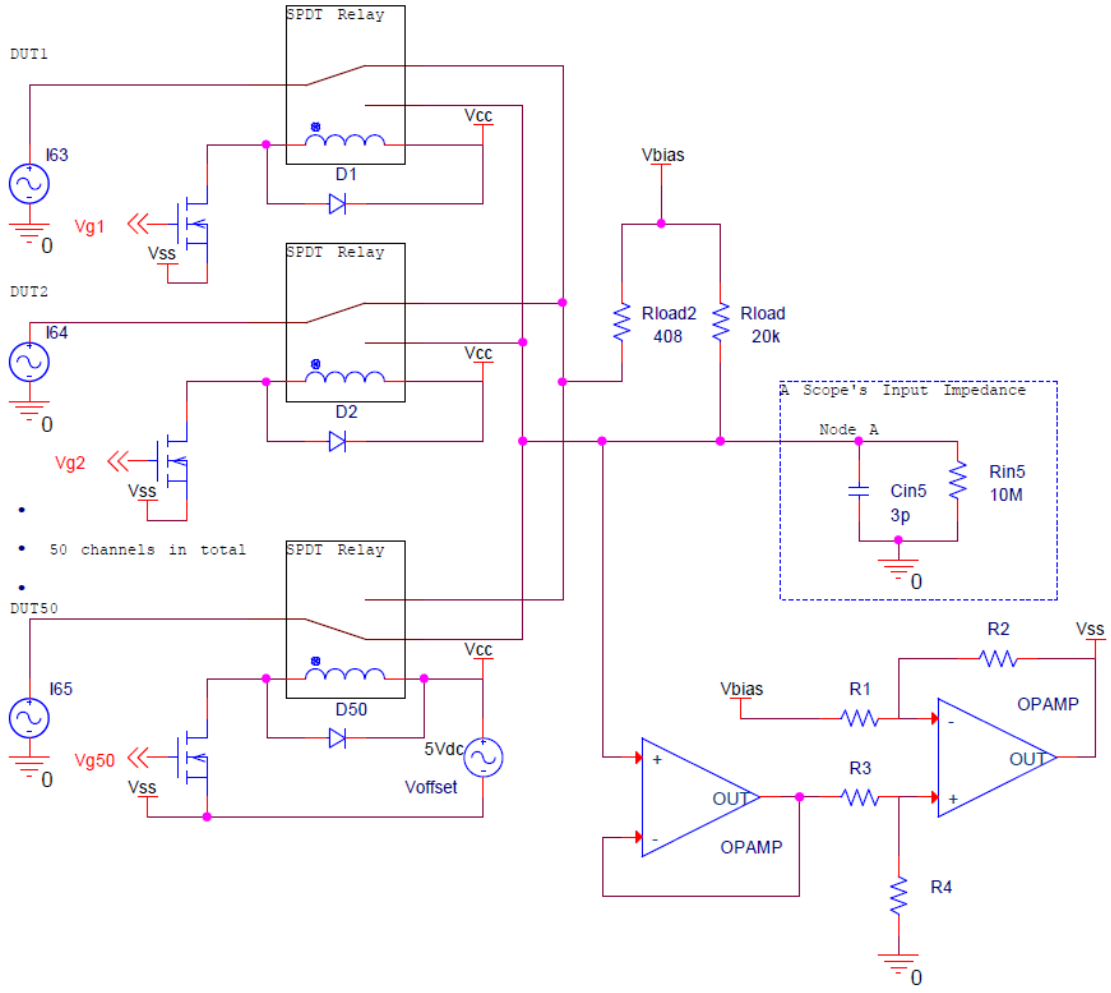

Figure 16 The overall solution to cancel reed relay mux parasitic capacitance

Summary

In applications where the impedance at a mux's common node is high, a high capacitance at the same node may limit the mux's bandwidth to below the frequency of interest. The techniques in this article can lower the parasitic capacitance of a reed relay mux to below a single relay's capacitance! The essence of these techniques is to drive the other side of parasitic capacitances with the same AC voltage as the common node. This can be achieved using op-amps, floating voltage sources, and/or simply a resistor. Besides extending bandwidth, these techniques can also be used in applications where a low capacitive load is desired, such as to stabilize amplifiers, test slewing behavior, and measure load step responses.

References

[1] Understanding Switch Topologies, NI white paper, Nov 10, 2015

[2] How to Choose the Right Relay, NI white paper, Nov 10, 2015

[3] What is a reed relay?, Graham Dale, Pickering Electronics (Part 1, Part 2)

[4] 9000 series reed relay datasheet, Coto Technology.

—Yong Liao received his BS and MS in EE in Shanghai Jiaotong University and University of California, Irvine respectively. He has been a R&D test engineer with Broadcom for 6 years.