

# EDN LEADING EDGE

WHAT'S HOT IN THE DESIGN COMMUNITY

EDITED BY FRAN GRANVILLE

## Runtime analysis tool probes your source code

Diab Data, a supplier of C and C++ compiler suites for the Motorola 68K, ColdFire, PowerPC, and MCore processor families, has developed visual runtime-analysis (RTA) tools that allow users to analyze their program's runtime behavior, implement optimizations, find memory errors, and configure memory layouts for their complex applications. RTA comprises a Visual Interactive Profiler (VIP); a Run-Time Error Checker (RTEC); and an interactive Link Map Analyzer, which provides multiple views of a developer's link map and allows interactive editing of memory setups. VIP provides block count and timing information and visual cues to help you locate the most heavily used source-code sections. The tool, which interacts with the embedded target, uses a counter or an interrupt tick to determine how long a processor spends in each function. Although this analysis technique provides a real-time evaluation, it imposes a small overhead on the executing application.

Once VIP collects the profile data, it interacts with the Diab Data compiler to invoke profile-driven optimizations. VIP also examines function-pair relationships at runtime and shows the percentage of time that one function called, or was called by, another (Figure 1). In addition, VIP shows



**FIGURE 1**  
VIP examines function-pair relationships at runtime and shows the percentage of time that one function called, or was called by, another.

how much time the program spends in each child function, depending on which parent function called it. Users can easily traverse the program hierarchy and uncover function-pair relationships, useful for analyzing calling patterns in

## EDN's Innovators of the Year bestow scholarship



By being selected *EDN's* 1996 Innovators of the Year, David Bingham (top left) and Charlie Allen (bottom left) of Maxim Integrated Products in Sunnyvale, CA, won the right to award a \$10,000 scholarship to the college or university of their choice. The engineers selected Northeastern University, and in a recent ceremony at the school's Boston campus, *EDN's* editorial director Michael Markowitz presented the \$10,000 Innovation check to the university's president.



Bingham and Allen won *EDN's* annual contest on the strength of their 13-year collaboration in designing innovative products for Maxim (see *EDN*, Feb 19, 1997, pg 37). *EDN's* panel of judges is now sorting through the nominations for the year's most innovative products and people and will present the finalists for your selection in the next issue of *EDN*.—by Joan Lynch



*EDN* Editorial Director Michael Markowitz (left) presents the \$10,000 donation to Richard Freeland, president of Northeastern University (far right); Allen Soyster, dean of Northeastern's College of Engineering (second from the left); and Arvin Grabel, chairman of Northeastern's Department of Electrical and Computer Engineering (second from the right).

complex applications. VIP also assists with code-coverage analysis to determine whether all portions of a program have been exercised. For code-coverage analysis, the compiler inserts one to three instructions in each function. Each time the CPU executes a function, the program writes to a designated memory area and increments a counter. VIP color-codes the original source text file, depending on its execution status.

The RTEC inserts test hooks into a user's program to aid

in its runtime analysis where it uncovers memory leaks, stack overflows, dangling or out-of-bounds pointers, and other memory-allocation errors that static program analysis cannot find. To minimize runtime overhead, you can specify which modules you want RTEC to analyze. Diab Data's introductory price for a node-locked license of the RTA Suite is \$450.—by Markus Levy

**Diab Data**, Foster City, CA. 1-415-571-1700, [www.ddi.com](http://www.ddi.com).  
**Circle No. 428**

## Quick FPGA conversion without NRE charges

If you have Altera (San Jose, CA) programmable-logic devices that you want to convert to ASICs, newcomer Clear Logic has a new way of getting you there. The company's laser-configured ASICs (LASICs) convert an FPGA design directly from a bit stream into an ASIC. According to Clear Logic, the converted device is functionally identical to the Altera part, including internal timing and pinout, eliminating any redesign or resimulation (although resimulating is always a good idea).

Rather than convert a coarse-grained FPGA architecture into a fine-grained gate array, each Clear Logic LASIC architecture matches an Altera FPGA-family architecture. Laser implementation of the LASIC devices eliminates photo masks, giving you prototypes in one week and production quantities in three to four

weeks. No mask cost also allows the company to eliminate NRE charges for your conversion.

According to Clear Logic, LASICs' use of laser fuses in place of the original



**Laser-configured CL8000 devices let you convert your Altera Flex 8000 FPGA designs into ASICs without NRE charges and one-week prototype time.**

FPGA's SRAM elements results in substantial power- and chip-size reductions—as high as 50% for each parameter. The company also claims that elimination of the SRAM programma-

ble elements also simplifies LASIC routing, which helps keep internal chip-timing paths equivalent to those on the FPGA. Clear Logic generates all test vectors for the converted design and guarantees 100% fault coverage.

LASIC devices support all six Altera configuration modes, allowing LASICs to be pin-compatible with the FPGAs they replace in all applications. You can currently get only the CL8000 family of LASIC devices for Altera Flex 8000 conversions. As an example of typical pricing, a 4000-gate CL8452A device in a 100-pin TQFP package costs \$10.40 (100). Clear Logic plans to introduce LASICs for other Altera families this year. (For additional information on FPGA-to-ASIC conversion, see "Moving beyond programmable logic: if, when, how?" *EDN*, Nov 20, 1997, pg 27.)—by Jim Lipman  
**Clear Logic**, Santa Clara, CA. 1-408-492-8585, fax 1-408-988-5632.

**Circle No. 429**

## Axial cooling fan cuts size, weight, noise

The DC 2406KL axial cooling fan from NMB Technologies weighs 45g, measures 60×60×15 mm, and offers 19- to 34-dB noise. Its target applications include chip-and-spot cooling



**Dual ball bearings impart long life to NMB's DC 2406KL series of miniature axial cooling fans.**

in Pentium-class notebook computers, set-top boxes, docking stations, and telephone packs. Variable-speed control allows you to select the optimum position for a speed-control sensor in your system to minimize fan noise and maximize cooling efficacy. The fan uses dual, preloaded, shielded ball bearings and meets all UL/CSA, VDE, and CE requirements. Models rated at 0.48 to 1.92W input power provide 0.19 to 0.52m<sup>3</sup>/minute airflow, respectively. NMB

guarantees the fans to be free of defects in materials and workmanship for 50,000 hours. Prices start at \$10.

—by Bill Travis

**NMB Technologies Inc**, Chatsworth, CA. 1-818-341-3355, fax 1-818-341-8207, [www.nmbtech.com](http://www.nmbtech.com).

**Circle No. 430**

## Memories deliver low-priced reprogrammability

If your design has moderate density requirements and requires the fast reprogrammability of flash, Macronix's multiple-time-programmable ROMs (MTPROMs) and Silicon Storage Technology's (SST's) many-time-programmable (MTP) flash may fill the bill. The memories offer lower cost than flash incurs for its ability to do thousands or millions of code updates. With packages and pinouts compatible with ROM, EPROM, and full-featured flash, the MTP devices also offer design flexibility.

Macronix's 1-Mbit MX26C1000A (128-kbit×8) and

MX26C1024A (64-kbit×16) and 512-kbit MX26C512A (64-kbit×8) provide a minimum of 100 reprogramming cycles—insufficient for data- and file-storage applications but often enough for infrequent code updates. Macronix has developed Paired Array Contactless AND, a 0.45- $\mu$ m process technology, which the company claims reduces die size and lowers cost. In addition, Macronix omitted other peripheral circuitry, such as blocking, voltage pumps, and automated state machines, from these initial MTPROMs to further reduce cost. The devices provide 5V access times as fast as 70 nsec, enabling direct execution in many 8- and 16-bit applications.

SST built the MTP flash on a thick-oxide, split-gate cell, identical to that in the company's full-featured SuperFlash products. Like Macronix, SST omitted most of the SuperFlash peripheral-circuit overhead, which in this case means that you have to program and erase the memories using an external programmer. SST claims a 1000-reprogramming-cycle specification. The company plans to offer a range of devices from 256 kbits through 4 Mbits, operating at 2.7 and 5V. Anticipated 5V access times are 55 nsec for the 256- and 512-kbit devices, 70 nsec for the 1-Mbit device, and 90 nsec for the 2- and 4-Mbit devices.

The MX26C1000A costs \$1.75 (1000) in 32-lead DIP/PLCCs and \$2.05 in 32-lead SOPs and TSOPs. The MX26C512A costs \$1.40 (1000) in 28-lead DIPs and 32-lead PLCCs and \$1.70 in 28-lead SOPs and 32-lead TSOPs. Both devices, plus the MX26C1024A in 40-lead DIPs, SOPs, and TSOPs and 44-lead PLCCs, are now in production. Macronix's future product plans also include lower voltage, extended temperature, single-voltage operation, and higher density MTPROMs.

The 1-Mbit (128-kbit×8) SST27SF010 is now available for sampling, and the company expects to begin volume production in April. Packaging options include 32-lead DIPs, PLCCs, and TSOPs, and the price is \$1.30 (100,000). Higher density MTP flash memories will offer compatible packages and pinouts, and packaging plans for the 256- and 512-kbit densities include 28-lead DIPs and TSOPs and 32-lead PLCCs.—by Brian Dipert

**Macronix America Inc**, San Jose, CA. 1-408-453-8088, fax 1-408-453-8488, [www.macronix.com](http://www.macronix.com). **Circle No. 431**

**Silicon Storage Technology Inc**, Sunnyvale, CA. 1-408-735-9110, fax 1-408-735-9136, [www.stti.com](http://www.stti.com).

**Circle No. 432**

## Inverter powers up multiple-CCFL backlights

The IB Series of dc/ac inverters from Endicott Research Group provides power for as many as 10 cold-cathode-fluorescent (CCFL) backlighting lamps. The power supplies contain the company's MT-Class inverter on a pc board that carries two mating out-

put connectors. Each connector can supply as many as five CCFLs. The inverters offer the option of onboard dimming circuitry. The IB Series inverter costs \$80 (OEM).

—by Bill Travis

**Endicott Research Group**, Endicott, NY. 1-607-754-9187, ext 3048, fax 1-607-754-9255, [www.ergpower.com](http://www.ergpower.com). **Circle No. 433**



**Get the maximum available brightness from your LCD, using a 10-CCFL dc/ac-inverter board.**

## CCD image sensor for PC-based video needs just one 5V supply

With the 1/5-in.-sq (0.5-cm-sq) LZ 2547 CCD sensor from Sharp Electronics, you can simplify power-supply requirements when building a videocamera for applications such as desktop videoconferencing, security monitors, and Internet and basic machine-vision systems. Unlike some CCDs, which require as many as four separate supplies, the LZ 2547 uses internal voltage generators to allow operation from a 5V, 4-mA supply. The one-supply approach cuts the size and the cost of circuitry associated with the camera. The sensor provides 362×582-pixel interlaced resolution, which is compatible with 352×288-pixel noninterlaced Common Intermediate Format (CIF) devices. It costs \$20 (1000).

—by Bill Schweber

**Sharp Electronics Corp**, Camas, WA. 1-360-834-2500, fax 1-360-834-8903, www.sharpmeg.com. **Circle No. 434**



The LZ 2547 CCD sensor offers single-5V operation for videoconferencing and monitoring applications.

## SPARC workstations target PC price points

Sun Microsystems has just rolled out a new family of low-end workstations based on the UltraSPARC Iii  $\mu$ P with prices that start at less than \$5000—squarely targeting high-end Wintel systems as competitors. The new Darwin family marks a transition by Sun to PCI-bus and other PC-I/O technologies for all desktop workstations, thereby helping the company to achieve lower prices. For example, the systems use IDE-based disk drives and CD-ROMs. Still, the Darwin workstations include Sun core logic, integrated 10/100BaseT LAN support, and an integrated graphics controller. A pizza-box-style Ultra 5 model based on a 270-MHz  $\mu$ P includes a 4-Gbyte disk, three PCI slots, and a minimum of 64 Mbytes of RAM and sells for less than \$5000. Moving up in performance, the Ultra 10 employs a 300-MHz  $\mu$ P, four PCI slots, and a tower case for less than \$10,000.

Sun has also adopted the PCI bus in higher end dual-processor systems. The new

Ultra 60 includes dual PCI buses—one 66-MHz bus supporting a single slot and a 33-MHz bus with three slots. The system supports the dual buses, dual 296-MHz  $\mu$ Ps, as much as 2 Gbytes of RAM, and dual graphics controllers with the 120-MHz UPA (UltraSPARC Port Architecture) crossbar interconnect. Prices for the Ultra 60 start at less than \$20,000.

The new systems mark a move by Sun to adopt PC technologies to compete with the high end of the PC market. In fact, Sun claims that users no longer need access to a PC because the company is offering both software simulation and PCI-based hardware add-in cards that allow SPARC systems to execute Windows applications. Meanwhile, however, the company has just signed a license deal with Intel (Santa Clara, CA) for access to Intel's 64-bit Merced  $\mu$ P that could mean that Sun plans to join Silicon Graphics (Mountain View, CA) and Hewlett-Packard (Santa Clara, CA) in offering Intel-based systems down the road.—by Maury Wright

**Sun Microsystems**, Palo Alto, CA. 1-415-960-1300, www.sun.com.

**Circle No. 435**

## A/D CONVERTER PROVIDES SYNCHRONIZED 14-BIT CONVERSIONS FOR POWER, PHASE ANALYSIS

When you're looking at phase-related information, such as in motor control or power-line monitoring, you need A/D conversions that are simultaneous across several channels. The MAX125 from Maxim provides 14-bit resolution on four channels at a maximum throughput group rate of 76k samples/sec. Four synchronized track-and-hold circuits within the device feed a single higher speed converter. Two multiplexed inputs precede each T/H circuit, providing a total of eight single-ended inputs. You can use the internal  $\pm 2.5$ V reference or an external reference for the converter.

The device stores conversion results in internal registers

that your system can access via a bidirectional parallel interface. Maximum conversion rate on a single channel is 250k samples/sec, and you can specify how many of the four channels you want included in the sampling; thus, the converter wastes no time sampling unneeded inputs. A sequencer in the IC manages the conversion process and indicates via an interrupt when the conversion cycle is complete; the next conversion cycle begins automatically. The  $\pm 5$ V-supply MAX125 is designed for a  $\pm 5$ V input range; the otherwise-identical MAX126 is scaled for  $\pm 2.5$ V inputs. Prices for the 36-pin SSOP devices begin at \$13.95 (1000).

—by Bill Schweber

**Maxim Integrated Products**, Sunnyvale, CA. 1-408-737-7600, fax 1-408-737-7194, www.maxim-ic.com.

**Circle No. 436**

## FPGA blue-plate special: extra memory, hold the cost

Xilinx's Spartan FPGA family follows in the low-cost trail blazed by the XC5200 product line. The company based Spartan on its 5V XC4000E devices, which offer an EDA-friendly, dual four-input-look-up-table, logic-block architecture but provide fewer long-line routing resources than do the higher gate-count XC4000EX/XL/XV products. With the goal of cost reduction, the Spartan architecture lacks the XC4000E's parallel-interface-configuration option and dedicated, on-chip, wired-AND decode structures. However, Xilinx retains the look-up-table-based select-RAM, which is not part of the XC5200 architecture. Other manufacturers of low-cost pro-

grammable-logic devices sometimes omit embedded memory.

Assuming that your design contains both logic and memory, estimated system gate counts range from 2000 to 40,000, targeting I/O performance as high as 80 MHz and with as many as 224 I/O pins. Xilinx also intends to cut prices by integrating on-chip BIST, thus reducing test time; and by using only low-cost test hardware and plastic packages, such as PLCCs, VQFPs, TQFPs, PQFPs, and BGAs. However, you need to keep low-power-design technique in mind to avoid thermal problems. Alliance and Foundation software v1.4, now shipping, support the Spartan product line, and both Xilinx and its AllianceCore partners already have extensive intellectual-property core support in place. Xilinx targets the end of the first quarter for availability

of its all-important PCI core.

The 5V, 20,000-gate XCS20; 30,000-gate XCS30; and 40,000-gate XCX40 are now available, and the XCS05 and XCS10 will follow in February. Prices range from \$3.95 (100,000) for the XCS05 to \$19.95 for the XCS40. By early in the third quarter, Xilinx will start shipping its lower cost and footprint-compatible 3.3V SpartanXL product line, beginning with 20,000- and 30,000-gate versions. The company has also recently introduced a second-generation PCI core and faster "-09" speed bin for its XC4000XL devices, as well as military-qualified versions and the 3.3V PCI-optimized XC4000XLT product line.

—by Brian Dipert

**Xilinx Inc**, San Jose, CA. 1-408-559-7778, fax 1-408-879-4780, www.xilinx.com. **Circle No. 437**

## Tool gives you early warning of design problems

Incases' EMC-Engineer lets you "look into" your pc-board design to check geometrical (layout), physical, and electrical parameters before and during board design. Electrical parameters available for analysis include trace-delay times, signal integrity, and electromagnetic radiation.

You use EMC-Engineer to simulate and analyze board-design decisions to guide subsequent com-

ponent placement and board routing.

A key to EMC-Engineer's ease of use is its ViewPorts feature. Each ViewPort presents a spreadsheetlike display of data in an ordered format. For example, the tool comes with a predefined ViewPort for signal integrity and another for pc-board physical data, such as per-layer copper thickness, dielectric constant, and trace angles.

You can also define your own ViewPorts for displaying data for a board design. Using a fast built-in signal-integrity simulator, you analyze waveform displays of some types of electrical data, such as signal overshoot and undershoot on selected nets.

You can use EMC-Engineer on partially and fully placed boards and on unrouted, partially routed, and fully routed designs. The tool runs on Windows NT- and Unix-based systems and has a starting price of \$15,950.

—by Jim Lipman

**Incases Engineering**, Fort Worth, TX. 1-817-332-7422, +011 44 1473 273300, fax 1-817-332-9226, +011 44 1473 274333.

**Circle No. 438**

Net Name	Impedance Discontinuity	Skew	Min Propagation Delay	Max Propagation Delay	Overshoot Type 1	Overshoot Type 2	Overshoot Type 3
PCPNet_01000	15.425	3.156	3.671	3.653	3.215	4.317	-0.282
PCPNet_01001	3.931	3.156	3.671	3.653	3.245	4.351	-0.235
EWNet_01000	15.425	3.156	3.671	3.653	3.324	4.314	-0.286
EWNet_01001	15.425	3.156	3.671	3.653	3.351	4.349	-0.245
DPNet_01000	15.425	3.375	3.914	3.359	3.171	3.227	-0.102
DPNet_01001	15.425	3.375	3.914	3.359	3.174	3.236	0.104
DPNet_01002	15.425	3.375	3.914	3.359	3.271	4.107	-0.204
DPNet_01003	15.425	3.375	3.914	3.359	3.273	3.226	0.102

EMC-Engineer's ViewPorts let you review data, such as signal-integrity parameters. The columns represent net name, impedance discontinuity, skew, minimum and maximum propagation delays, and three types of signal overshoot.

**Subminiature MOSFET relays suit PCMCIA systems**  
Measuring only 4.2×6.5×2.1 mm, the G3VM solid-state-relay family from Omron has a low enough profile to fit onto PC Cards in PCMCIA systems. The MOSFET-based relays are available in four-, six-, and eight-pin versions. They offer a variety of continuous-load current connections—ac, dc single, and dc parallel—at 120, 150, and 200 mA. G3VM relays spec output voltages to 350V dc, 50-mA input current, -350 to +350V output-load voltage, and maximum load resistance of 35Ω. The devices are available in industry-standard surface-mount and through-hole configurations. Prices start at \$1.35 (1000).—by Bill Travis  
Omron Electronics Inc, Schaumburg, IL. 1-800-556-6766, fax 1-847-843-8081.

Circle No. 439



**MOSFET technology paves the way for IC-size relays that fit into tight PCMCIA quarters.**

## Application notes help you to not repeat others' mistakes

Design engineers are drowning in electronic-component information, such as IC data sheets and vendor application notes. Application notes help you use an effective design-in device, minimize frustration, and prevent you from reinventing the wheel. A free, vendor-independent searchable database from QuestLink Technology can ease your awareness of and access to these sources of valuable information.

The cross-referenced database includes notes from more than 200 manufacturers and requires you to know neither the vendor name nor the part number. QuestLink based the database on subject key words from the note's contents, not simply on the title of the note, which can be misleading or incomplete. Standard subjects include topics such as PLDs, SCSI, RS-232C, MPEG, JTAG, flash, wireless, and 8051.

The QuestLink application-note database adds to the company Web site's EEDesign Center, a free, central source for IC-product information from many vendors. A proprietary search engine on the site allows engineers to look for ICs by vendor, part number, function, key words, and similar criteria. The company has also announced an alliance with distributor Hamilton Hallmark. This alliance allows you to electronically order even small quantities of parts, so that you can quickly go from the device-selection stage to evaluating the component in your prototype.—by Bill Schweber

**QuestLink Technology Inc**, Austin, TX. 1-512-322-3220, fax 1-512-322-3132, [www.questlink.com](http://www.questlink.com).

Circle No. 440

## CALENDAR

### Feb 5 to 7

**International Solid-State Circuits Conference**, San Francisco, whose theme is global communications, offers tutorials on op amps, solid-state relays, clocks, SRAM, microelectrical-mechanical systems, and finite-impulse-response. Each tutorial costs \$60. Registration costs \$390 for IEEE members and \$465 for nonmembers. Courtesy Associates, Washington, DC. 1-202-973-8667.

### Feb 9 to 13

**Wireless Symposium and Portable by Design**, Santa Clara, CA, combine to present 50 workshops, conference sessions, keynotes, and a design-engineering trade show. Topics include battery basics; active-, digital-, and RF-filter design; wireless made simple; CPUs and DSPs for portable devices; IC options; mobile-system packaging; point-to-point and base-station design; wireless LANs; and personal-communications services. More than 250 manufacturers showcase hardware, software, services, and test equipment for the wireless and portable-electronics markets. All-inclusive registration costs \$898 on or before Jan 23 and \$1010 on or before Feb 13. Penton, Hasbrouck Heights, NJ. 1-201-393-6286.

### Feb 9 to 13

**Software Development '98 Conference**, San Francisco, features classes, lectures, and product announcements. You can choose between managing-software-development tracks and hands-on tutorials in Java and C++. Software-development classes cover 12 technical areas, from language studies in Java and C++ to user-interface design. A software-development expo features hundreds of vendors and tools. Miller Freeman, San Francisco, CA. 1-415-905-2702.