

# DSP IC's clock oscillator uses inexpensive crystals

SERGEY DICKEY, DYNAMIC TELECOMMUNICATIONS INC, GERMANTOWN, MD

## Circuit tricks eliminate a DSP chip's need for expensive, low-ESR crystals.

The internal clock-oscillator circuit in the TMS320C50 family of DSP chips from Texas Instruments (Dallas) normally requires low-ESR (effective series resistance) crystals for reliable operation. The IC's data sheet (Reference 1) cites  $30\Omega$  maximum for this parameter. However, the maximum ESR spec for crystals from several manufacturers is approximately  $80\Omega$ . Even worse, measurements show that  $R_s$  exceeds the specified value by as much as 50 to  $60\Omega$  in as many as 11% of the units under test. Moreover, even with crystals whose ESR is lower than  $30\Omega$ , the oscillator's gain margin can be dangerously low for oscillation frequencies approaching 60 MHz. The circuit technique provided here allows you to safely use inexpensive crystals with relatively high ESR.

The reason for these DSP chips needing low-ESR crystals is their relatively low high-frequency gain, along with the low input resistance of the CMOS inverter in the oscillator circuit. Figure 1 shows the manufacturer's recommended clock circuit. Here, the inverter which uses a resistor in a negative-feedback loop for biasing creates approximately  $180^\circ$  phase shift. The external circuit must provide an additional  $180^\circ$  at the series-resonant frequency of the crystal. Oscillation begins if the circuit meets the Barkhausen criterion the initial loop gain at the frequency of zero phase shift exceeds unity. The value of the gain at this frequency is the gain margin; this value provides a useful measure of the oscillator's robustness.

The sequence of events leading up to this design started during the prototype stage of a wireless-product development project, when many new SMT crystals failed to oscillate in the TMS320C50-57 clock circuit. Those crystals that did oscillate caused crashes after several hours of operation. The circuit used third-overtone crystals with a nominal series resonant frequency of 56.32 MHz. Table 1 provides the small-signal parameters of the internal oscillator circuit in the DSP chip, as measured at 56.32 MHz with a network analyzer. The values agree with the

parameters given in Reference 2; however, Reference 2 does not discuss the inverter's input resistance.

The crystal-resonator model uses a measured  $17.6\Omega$  ESR value of a good resonator. By choosing a  $10^5$  typical Q value, you can obtain both the crystal's inductance and motional capacitance. You can also obtain the crystal holder's capacitance either from the manufacturer's data sheet or from mea-

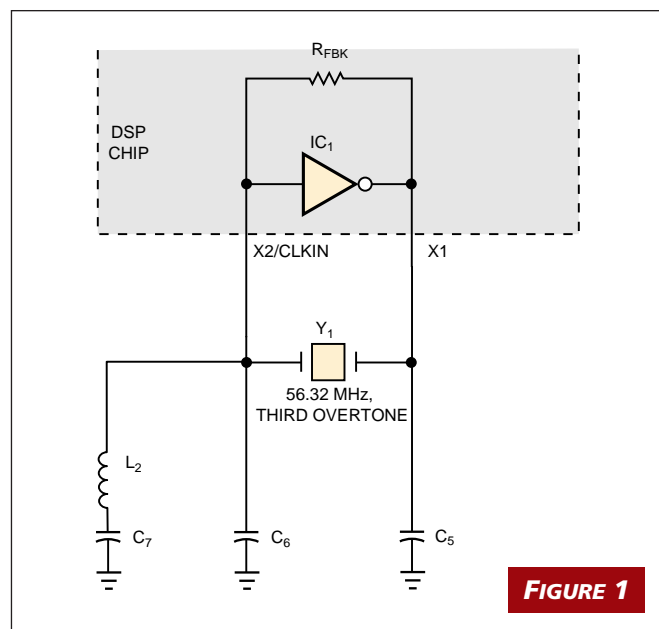


FIGURE 1

This configuration, recommended by the DSP-chip manufacturer, has insufficient gain margin with high-ESR crystals.

**TABLE 1—INTERNAL-OSCILLATOR CIRCUIT PARAMETERS AT 56.32 MHz**

Parameter	Measured value
Gain in $50\Omega$ circuit	5.7 dB
Phase shift	140
Input impedance	$198\Omega$ in parallel with $17.3\text{ pF}$
Output impedance	$261\Omega$ in parallel with $7.9\text{ pF}$

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surements. For higher resistance crystals, resistance is the only parameter that changes in this model. Table 2 lists the parameters of the computer simulation. The simulation of the oscillator circuit's open-loop parameters uses Spice's ac-analysis mode.

Figure 2 shows the full schematic of the open loop. The block comprising gain stages  $E_1$  and  $E_2$ , phase shifter  $R_1-C_1$ , output section  $R_2-C_2$ , and input section  $R_5-C_8$  represents the circuitry internal to the DSP chip. Because the oscillator is normally a closed loop, the input section loads the circuit's output in this open-loop representation. Measurements and a separate simulation in a  $50\Omega$  circuit verify the internal model. Another block, comprising  $L_1, C_4, R_3$ , and  $C_3$ , represents the crystal. Finally, the series-resonant circuit formed by  $L_2, C_7$ , and  $R_4$  prevents the real-life circuit from oscillating at the fundamental frequency. Points A and B show the location of inductor insertion.

The goal was to find optimal values of external components providing best gain margin for varying values of crystal ESR. Both simulation and experiments showed that the values of the two external phase-shifting capacitors must be fairly large to maintain oscillation with crystals having moderately high ESR. As

TABLE 2—CRYSTAL MODEL

Parameter	Value
Series-resonant frequency	56.32 MHz
Q	$10^5$
Series resistance	17 to $150\Omega$
Inductance	4.97 mH
Motional capacitance	$1.61 \times 10^{-15}F$
Shunt capacitance	$5.1 pF$

FIGURE 2

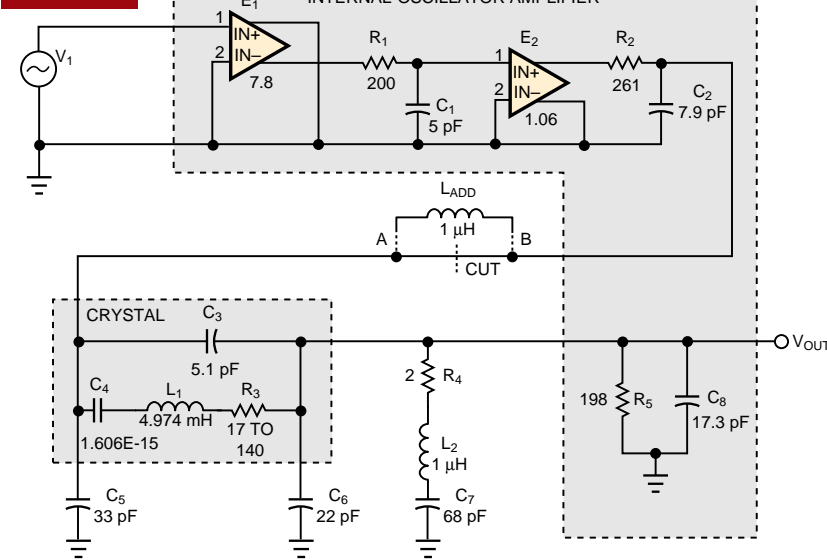


TABLE 3—GAIN MARGIN VS CRYSTAL RESISTANCE

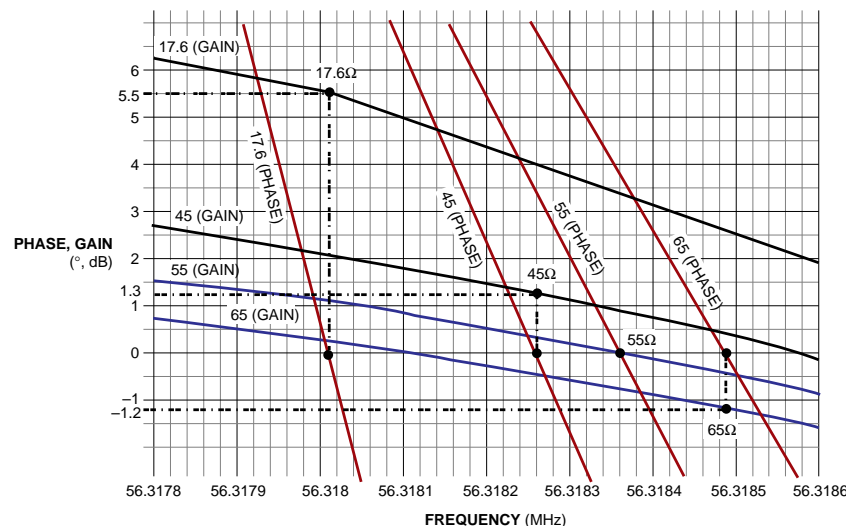
Series resistance ( $\Omega$ )	Gain margin (dB)
17.6	5.5
45	1.3
55	0
65	1.2

TABLE 4—GAIN MARGINS WITH SERIES INDUCTOR ( $L=1 \mu H, C_5=9 pF, C_6=8 pF$ )

$R_s$ ( $\Omega$ )	Gain margin (dB)
17.6	7.0
45	6.0
60	5.4
70	5.0
80	4.6
100	3.8
120	2.7
140	1.1

Spice simulation yields this equivalent circuit of the TMS320's oscillator circuitry.

FIGURE 3



Spice analysis of the circuit in Figure 3 produces these phase and open-loop-gain response curves.

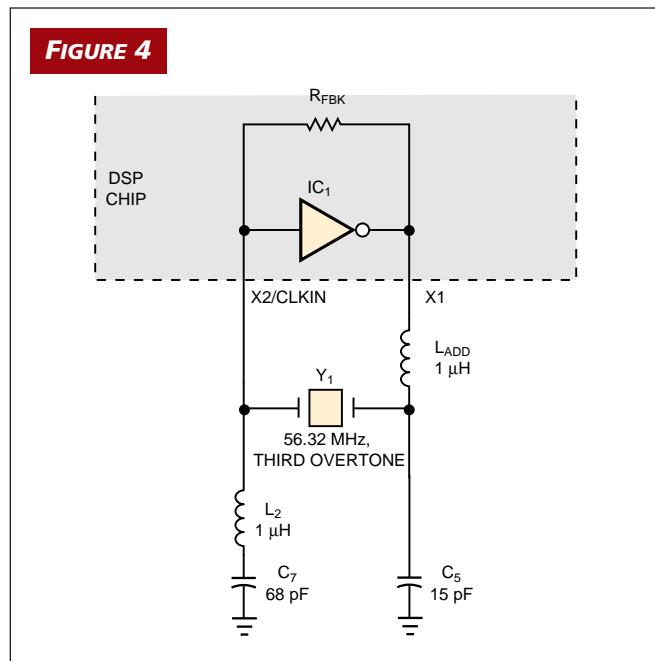
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an example, Figure 3 shows the results with the component values in Figure 2 (no  $L_{ADD}$ ). Here, the group of mostly vertical lines comprises open-loop phase responses, whereas the more horizontal lines are the corresponding open-loop gains, with series resistance as a parameter. To find a gain margin, find the frequency where the phase-response curve crosses the  $0^\circ$  line, then look up the value of the corresponding gain curve at the same frequency. Table 3 summarizes the results from Figure 3.

For values of  $R_s$  lower than  $30\Omega$  in the range that TI recommends, a healthy margin exists; but for higher values the oscillation is either shaky or impossible. This simulation prediction correlates well with experimental results. Attempts to find significantly better values of external components were unsuccessful, apparently because it is necessary to increase the values of phase-shifting capacitors  $C_5$  and  $C_6$  to bring the loop phase shift to the required zero value. Such increases, however, reduce the value of the loop gain in this RC circuit.

A little coil will do it

Experiments showed that by inserting an inductor in series with the crystal (between points A and B in Figure 2), it is possible to realize a much greater phase shift without increasing capacitance to the level that brings the gain down to 0 dB. Even a small inductance helps to increase gain margin. For example, 100 nH yields a gain margin of greater than 1 dB in a circuit with  $60\Omega$   $R_s$ . Table 4 summarizes simulation results. A production run that used crystals with  $R_s$  as high as  $55\Omega$  confirmed the improvement shown in Table 4. Not a single crash has occurred since inductor insertion. Figure 4 shows the schematic of the modified oscillator circuit. Note that  $C_6$  is missing, and increasing  $C_5$  (relative to the simulation value) takes care of the phase shift.



The addition of  $L_{ADD}$  improves the oscillator's gain margin and eliminates the need for  $C_6$  to boot.

## References

1. TMS320C5x, TMS320LC5x Digital Signal Processors, Data Sheet SPRS030A, Texas Instruments, April 1995.
2. Turner, Clay, Use of the TMS320C5x Internal Oscillator with External Crystals or Ceramic Resonators, Application Report SPRA054, Texas Instruments, October 1995.

## Author's biography

Sergey Dickey is director of engineering at Dynamic Telecommunications (Germantown, MD), where he designs and develops cellular-communications equipment. His designs include a wireless local-loop terminal and a high-speed scanning test receiver. A member of the IEEE Communications Society, Dickey received an MSEE degree at the Moscow Physical-Technical Institute.

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