

Interface issues deter faster adoption of flat-panel displays

MANJU NATH, TECHNICAL EDITOR

Flat-panel displays are getting ready to replace CRTs as the display of choice in desktop PCs. However, take time before designing your system to select the optimum analog or digital interface to drive FPDs from the PC.

Flat-panel displays (FPDs) continue to offer an increase in color depth and resolution, both of which are equal to or better than CRT image quality. But interfacing high-resolution FPDs to PCs is becoming a tough design issue. Thanks to an ever-increasing data rate required to support high-resolution FPDs, EMI (electromagnetic interference) is becoming a major consideration (Table 1). In addition, you can no longer rely on a simple parallel-pin ribbon cable, such as a standard 15-pin RGB connector, because of an increasing number of lines in the ribbon cable. For example, you need 12 data lines to support SVGA 64,000-color panels but 36 data lines to support XGA 256,000-color panels. This constraint effectively rules out the possibility of standardizing connectors for FPDs with varying resolutions.

Designers currently have two choices in connecting an FPD to a PC: First, they can use the conventional CGA or analog signaling, and, second, they can use a digital transmission/signaling, which is available from National Semiconductor, Silicon Image, and Texas Instruments.

First-generation LCD monitors relied on an analog interface from the PC. They did so by taking analog video out of the RAMDAC in the VGA and then transmitting to a receiver where the signals were converted back to digital using A/D conversion. (The FPD monitor interface was digital.) But this scheme of using existing graphics-controller cards leaves you with a few problems. Because CRTs are analog devices, they are relatively tolerant of timing variations. But FPDs, as digital devices, are intolerant of even fine timing variations. For example, in an active-matrix LCD, each pixel is individually addressed and continuously driven. Analog-signal sampling errors resulting from using DACs in graphics-controller cards cause image distortion in space, time, and gray scale. Also, in a high-speed analog-signal transmission path, noise and distortion accumulate and lead to further image degradation.

TABLE 1—DATA-RATE TRENDS FOR FPDs

Graphics standard	Resolution (pixels)	256 colors (Mbytes/sec)	64,000 colors (Mbytes/sec)	16.7 million colors (Mbytes/sec)
VGA	640×480	25	50	75
SVGA	800×600	40	80	120
XGA	1024×768	65	130	195
SXGA	1280×1024	108	216	324
UXGA	1600×1200	162	324	486

Note: Estimated data rates courtesy Silicon Image.

INTERFACING FLAT-PANEL DISPLAYS

National Semiconductor's RSDS (reduced-swing differential-signaling) technology uses LVDS (low-voltage differential signaling), a technique that restricts voltage swing level to 100 mV to help reduce power consumption and minimize EMI levels in TTL-level signaling on the bus (Figure 1). The FPD63310 timing controller resides on the TFT (thin-film-transistor) LCD panel and provides the data buffering and control-signal generation for the FPD (XGA and SVGA). With integrated RSDS transmitters, the device feeds the LMC7532 column drivers at 130 Mbps with a 65-MHz clock. Operating at a 65-MHz clock frequency enables a single-pixel system interface, eliminating one of the two pixel buses typically required in TTL-type panels.

Connecting the FPD63310 timing controller and the LMC7532 column driver, the RSDS bus comprises nine differential data lines and the clock line from the timing controller. The narrow nine-pair RSDS column driver bus minimizes the width of the pc board on the LCD panel. The LMC7532 column driver incorporates an RSDS receiver and demultiplexer, registers, latches, and output drivers. The device converts the 18-bit RSDS digital data into analog voltage using an accurate (± 5 -mV), switched-reference-type DAC with low

reference current for the selectable groups of 300 or 309 columns in SVGA or XGA systems. For example, because an LMC7532 has 309 outputs, you would need 10 LMC7532s to address an XGA panel (1024×3 pixels/309). The LMC7532CT column driver, which costs \$6.50 (10,000), comes in a TCP (tape-chip package) with dual leads that connect to the panel pc board and glass. The FPD63310 comes in a 100-pin TQFP and costs \$8.50 (1000).

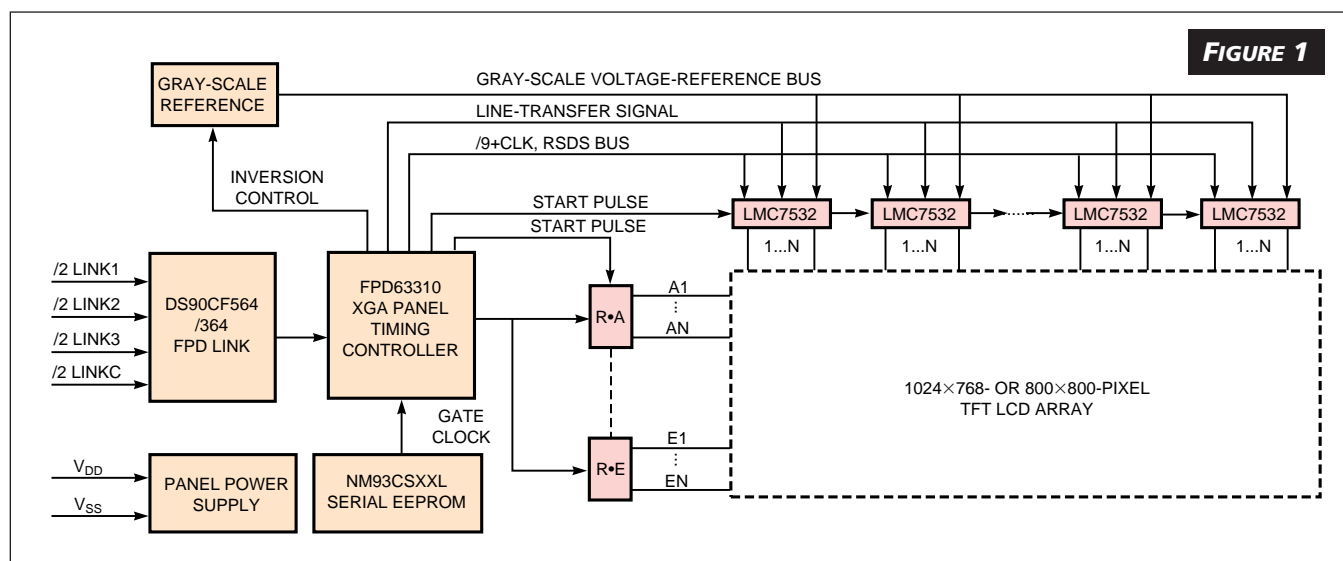
Digital interface needs encoding

Though it works well in solving EMI problems and limiting power consumption, LVDS has its drawbacks, too. First, LVDS requires additional channels to support higher resolutions above XGA; second, it has no encoding/decoding scheme. Data is simply latched relative to the clock edge at the receiver, which makes LVDS sensitive to cable skew with a 250-psec typical skew tolerance. This move limits the distance of video-data transmission to 10m if you use LVDS. PanelLink, which Silicon Image developed, is a data-transmission protocol that uses both LVDS techniques and a proprietary 8B/10B encoding scheme to improve serial-digital-data transmission (Figure 2). The lower voltage and encoded signals generate less EMI, eas-

ing the job of the system designer.

The PanelLink protocol defines an industry-standard interface that transfers data, clock, and control signals from the host LCD graphics controller to high-resolution, high-color FPDs at distances greater than 50m. The interface aims to address LCD-panel-interface problems, such as increasing clock rates, number of data lines, and cable length, all of which affect today's advanced FPDs. PanelLink technology implements the Video Electronics Standards Association (VESA) transition-minimized differential-signaling (TMDS) standard over a well-defined scalable architecture on industry-standard CMOS technology.

TMDS accepts 24-bit data with 8 bits for each color: red, green, and blue. An innovative encoding scheme dc-balances data and permits transmission of additional control signals without the need for separate control lines. Each byte of data is encoded into 10 bits with two added prefix bits to indicate the condition for dc-balance and transition minimization. The main benefit of the TMDS encoding/decoding scheme is to use the clock as a frequency reference, not for latching data. This technique allows each color channel to act independently, ensuring high-skew tolerance—as much as one clock cycle (15



The DS90CF564 LVDS receiver converts LVDS signals back into 21 bits (18 bits of RGB data plus 3 bits of LCD timing and control data) of CMOS/TTL data. The FPD63310 timing controller uses this data to drive both column and row drivers on XGA and SVGA TFT LCD panels.

INTERFACING FLAT-PANEL DISPLAYS

nsec for XGA)—and allowing cross-compatibility from process geometry to process geometry and from fab to fab.

The TMDS encoding algorithm performs dc balancing, which ensures a minimum number of transitions in the differential signal (to reduce the effective data frequency on the differential data lines) by inverting some data bytes to balance the number of ones and zeros. The interface requires only three data channels (RGB) and a clock channel. The three TMDS channels can transfer data as fast as 1.12 Gbps per channel. A programmable internal termination impedance enables optimum match, which is crucial for high-speed signaling.

In June, VESA ratified Plug&Display, a standard based on Silicon Image's PanelLink. Plug&Display regulates digital transmission of digital video signals from a graphics card to the flat-panel monitor. The standard stipulates a transmission protocol, cable design, connector design, and extensions to the DDC (display data channel) for timing-data exchange.

Silicon Image's Sil140/141 transmitter/receiver pair uses TMDS encoding to eliminate separate control-signal lines and transfers as many as 24-bit/pixel/clock cycle inputs and 24-bit/pixel/clock cycle outputs. The devices support as many as 16.7 million colors in resolutions from VGA through SVGA. A sync-detection circuit supports VESA P&D Hot plugging. The Sil140 is available in a 64-pin TQFP; the Sil141 comes in an 80-pin TQFP. The Sil140 and 141 cost \$14/pair (1000).

Brian Underwood, marketing vice president at Silicon Image, notes that an analog interface keeps overall system costs high, insisting that an all-digital interface is the best way to drive an FPD. He estimates that the average cost of an analog interface would amount to \$300 (compared with a \$50 average cost for the digital interface).

Underwood says, "You

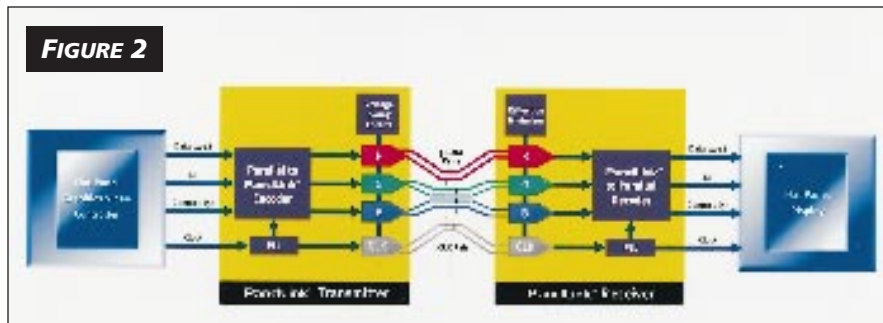


Figure 2 PanelLink accepts 24-bit data with 8 bits each for red, green, and blue. Each 8-bit group converts to 10 bits with two added prefix bits to indicate the condition for dc balance and transition minimization.

need PLL, three ADCs, a timing-control ASIC, and cable connectors for interfacing FPDs to PCs, whereas a digital interface needs only a transmitting/receiving pair and standardized cable and connector." Underwood also notes that scalability is a major problem with higher resolution FPDs, requiring expensive DACs in the VGA, which, in turn, necessitates new technology at a greater cost if you are using an analog interface.

But Vijay Desai, marketing vice president at Sage Inc, a display interface-electronics board maker, disagrees. Although PanelLink may be an interesting technology, it is still expensive, he claims.

"PanelLink is an LVDS-based interface. But this interface comes at a price. You need a PanelLink transmitter and receiver on a PC and an FPD, respectively. This situation means that you need a new graphics-controller card, and LCD vendors need to license PanelLink receivers. So you have a price/performance issue," notes Desai.

Desai says you instead need to offer both analog and digital connection to an FPD for easy technology migration. Sage offers the \$199 (10,000) Cheetah monitor board for VGA to XGA resolutions (Figure 3). The 5×6-in. board supports 16.7 million colors for TFT panels and provides 262,000 colors for CSTN (color super-twist nematic) panels. Cheetah also accepts LVDS or PanelLink signals. To accommodate this option, Sage provides a daughtercard with embedded LVDS or PanelLink receivers, helping you bypass the analog portion of the board. Using SureSync, a firmware feature, Cheetah can automatically detect VGA through XGA modes. The board's firmware also offers a customized on-screen display menu as an OEM vendor specifies. A proprietary ASIC detects incoming signals for resolution and refresh rate and then reacts in real time. The board conforms to VESA-DDC1/2B display ID for plug-and-play operation and supports TFT and CSTN panels from major LCD-panel vendors.

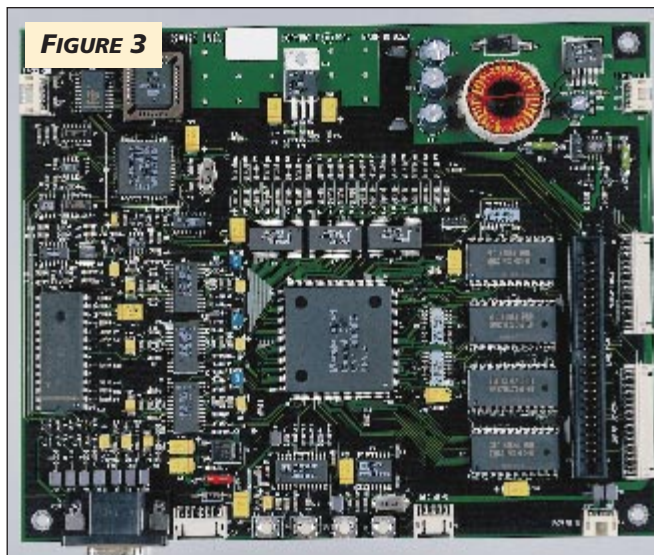


Figure 3 The 5×6-in. Cheetah board accepts analog RGB input through a standard DB15 connector with separate VSYNC and HSYNC, just like a CRT monitor. Onboard frame-rate conversion firmware supports VGA to XGA resolutions.

INTERFACING FLAT-PANEL DISPLAYS

According to Desai, even an all-digital interface cannot guarantee that all FPDs can work using PanelLink, because FPDs come integrated with driver electronics, which may lead to subtle timing variations.

"LCD panels change from vendor to vendor because the LCD panel is a module with drivers from possibly vendors such as Vivid (San Francisco), TI, National, Supertex (Sunnyvale, CA), and Cirrus Logic (Fremont, CA). Even LCD notebook panels don't work; some difference in panel impedance always shows up, which leads to image-quality degradation. Applying that same theory, driving the LCD monitor digitally is going to be difficult because it still gets digital output from the PCI bus," says Desai.

To address timing variations among FPD vendors, National has made several innovations to its timing-controller circuit. For example, using the NM-93C56L serial EEPROM, you can program the FPD63310 timing controller to

adjust for optimal display quality in real time by modifying the panel's timing signals. This programmability enables quicker time to market than the more common gate-array approach, which takes a few weeks for modification. Also, scaling and multisync detection are difficult in interfacing FPD panels.

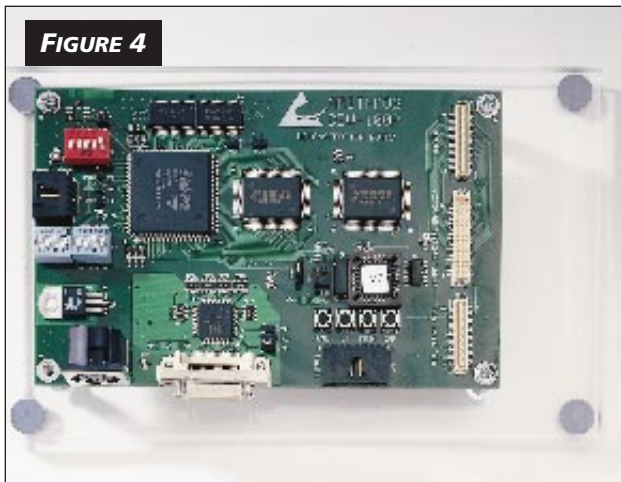


FIGURE 4
The Arithmos DEV 100P demonstration board accepts digital video encoded in TMDS format through the 3M (Maplewood, MN) 26-pin MDR connector. The onboard SiL101 PanelLink receiver IC decodes the encoded digital video. Then, the Arithmos ADE100 Display Engine converts the 24-bit digital TFT-style video stream generated by the SiL101 into the properly formatted STN stream.

Says Desai, "LCDs are fixed-resolution devices having a specific number of precisely fabricated pixels. To be compatible with a graphics subsystem configured for a different resolution, you need a scaling engine needs to be used to resize the image data to the resolution of the LCD."

Development boards

Silicon Image claims that Trident (Mountain View, CA), Hyundai (San Jose, CA), LG Semicon (San Jose, CA), Intel, Cirrus Logis, and Sharp (Sunnyvale, CA) have licensed the PanelLink transmitting core for integration into video-graphics controllers. Two companies have adopted Silicon Image's technology in their products. For example, Buffalo offers FPDs it bases on Silicon

Image's technology. The Buffalo FTD-XT13-PL, a 13.3-in. active-matrix TFT panel, supports XGA resolutions and TMDS PanelLink with a VESA Plug&Display connector. Note that you need a PCI-based graphics-card WGP-VG4MX-PV from Buffalo to drive the FTD-XT13-PL panel.

Rob Soderbery, marketing vice president at Arithmos Inc, says specialist ASICs are a necessity in driving FPDs with PanelLink technology.

"If you have a graphics controller, you cannot drive a flat-panel monitor directly from the graphics controller. You need additional support, which is why we provide the ADE graphics engine," says Soderbery.

Arithmos offers the ADE100 and the ADE200 FPD-controller ASICs. Both devices reside on a monitor card inside the FPD and provide STN grayscale control, display refresh, panel-timing generation and control, and scaling and multisync support. The ADE100/200 incorporates the PerfectColor algorithm, which provides true-color performance and eliminates traditional passive-matrix LCD artifacts, such as spatial errors and temporal artifacts such as "flicker" and "swim." The ADE100 graphics engine works with VESA Plug&Display-based FPDs. Fur-

FOR MORE INFORMATION...

For more information on products such as those described in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you read about their products in EDN.

Arithmos Inc
Santa Clara, CA
1-408-982-4480
fax 1-408-982-4481
www.arithmos.com
Circle No. 315

Buffalo Inc
Salem, OR
1-503-585-3414
fax 1-503-585-4505
www.buffinc.com
Circle No. 316

National Semiconductor
Santa Clara, CA
1-408-721-4962
fax 1-408-721-7321
www.national.com
Circle No. 317

Sage Inc
Santa Clara, CA
1-408-748-0500
fax 1-408-748-8540
www.sageinc.com
Circle No. 318

Silicon Image Inc
Cupertino, CA
1-408-873-3111
fax 1-408-873-0446
www.siimage.com
Circle No. 319

Texas Instruments
Dallas, TX
1-800-477-8924, ext 5300
www.ti.com
Circle No. 320

VOTE ...
Please also use the Information Retrieval Service card to rate this article (circle one):
High Interest 590
Medium Interest 591
Low Interest 592

Super Circle Number

▶ For more information on the products available from all of the vendors listed in this box, circle one number on the reader service card.

Circle No. 321

INTERFACING FLAT-PANEL DISPLAYS

ther, the ADE200 incorporates a proprietary algorithm, which eliminates the effects of a noisy signal found on an analog RGB monitor interface. Arithmos claims that the ADE100/200 supports STN LCD panels from all major Japanese STN manufacturers, including Sharp (Kyoto), Hitachi (Tokyo), Sanyo (Tokyo), Kyocera (Kyoto), and Matsushita (Osaka).

To ease FPD interface development, Arithmos offers ADE100/200 evaluation boards with socket support for both LVDS and PanelLink technologies. For example, the \$1049 DEV100P is an evaluation board with cable and connectors for the ADE100/200 devices (Figure 4).

Opinion is still divided on FPD interfacing. Soderbery admits that the FPD interface situation is fluid.

“Digital connection people are going digital by connecting the frame buffer of the PC directly to the digital flat-panel monitor for better connection,” he notes. Further complicating the situation are monitor vendors, which are in no hurry to commit themselves to any standard. “There is no standard. There is a debate going on,” says Soderbery. “The people producing monitors are simply using an analog standard. People working with digital standards are in two major camps—Silicon Image vs National and TI. Analog monitors will remain popular. The second generation needs to support both digital and analog for some time.” ☐

You can reach Technical Editor Manju Nath by phone +852-2965-1534, fax +852-2976-0706, or via e-mail at nsmanjunath@cahners.com.hk.

VOTE

Please use the Information Retrieval Service card to rate this article (circle one):

High Interest	Medium Interest	Low Interest
590	591	592