

# Use logic-analyzer setup/hold triggering to ensure timing margins

COLIN L SHEPARD, TEKTRONIX INC

As digital-system designs operate at ever-higher speeds, engineers must take greater care to ensure timing-margin adequacy. If your logic analyzer offers setup/hold triggering, you can take advantage of the capability to perform this essential characterization. By using techniques based on logic-analyzer triggering, you can efficiently characterize timing, even in fast, complex circuits, and release designs to production confident that those designs have sufficient timing margins.

## Can't overlook timing margin

You can no longer rely on the presence of enough margin in component specifications to accommodate the full range of system-design variation. Because they push performance to the limits of technology, component manufacturers can't provide much margin. For example, memory manufacturers' standard practice is to test and sort devices by speed and to sell ICs based on actual device performance. Although this approach allows the industry to harness the most that technology can offer, it effectively "tests out" components' timing margins, regardless of the specified speed.

Evaluation of prototypes' timing margins is therefore becoming critical. It may be tempting to save time and money by skipping this effort and to rely instead upon component specifications. Yet, because of the high cost of systems reaching production without enough margins, such an approach is no longer practical. Unfortunately, as they get faster, digital systems are also becoming more complex. So, as they discover that creating reliable designs requires greater effort on timing verification, engineers are also finding that they must pay attention to more signals. Given these realities, how do you effectively and efficiently perform the critical evaluation of timing margins?

The essence of a digital system's timing margin is

With a logic analyzer that offers setup/hold triggering, you can easily measure system timing margins. Straightforward examples explain how to do it.

setup/hold time. Timing margin is the difference between a design's actual and required setup/hold times. Variations in delays determine the margin in any system.

Timing-margin challenges exist in every digital system. A common example is the simple use of memory devices. Because it drives a number of devices, the write-enable, or clock, line is typically loaded more heavily than the address or data lines. This situation results in a longer propagation delay for the write-enable/clock line, which in turn results in less hold time. For RAM components, hold time often has little or no margin, so even the normal and intended uses of memory devices can create a timing-margin challenge.

## Assess timing margin

The large number of signals in modern systems amplifies today's timing-margin challenges. Fortunately, a logic analyzer with setup/hold triggering can simultaneously measure timing margins on many digital signals. To take advantage of this feature, you can connect the logic-analyzer probes to memory-device pins and the logic analyzer's clock input to the memory-write-cycle control signal. The logic analyzer uses this external clock, which may be an SRAM write-enable or a synchronous-DRAM clock. This connection allows the logic analyzer to view the memory-bus signals just as the RAM device views them.

Next, you establish the trigger setup. You program the logic analyzer to trigger on a setup/hold fault, and you define the violation according to the signals you are characterizing. The trigger setup programs the logic analyzer to check the 32-bit memory-data bus against a RAM setup/hold specification of 3.5 nsec/1.5 nsec. The logic analyzer measures the setup/hold time at the analyzer's inputs. If the signals ever violate the defined requirements, the logic analyzer triggers and captures the bus activity before

## TIMING-MARGIN MEASUREMENT

and after the fault.

With a solid design, the logic analyzer should never trigger under these conditions because signals should never violate the RAM setup/hold specifications. To learn what timing margin is present, you can take a series of logic-analyzer acquisitions with different setup/hold triggering values. *Figure 1* depicts a sequence of steps that you can follow to characterize the timing margin.

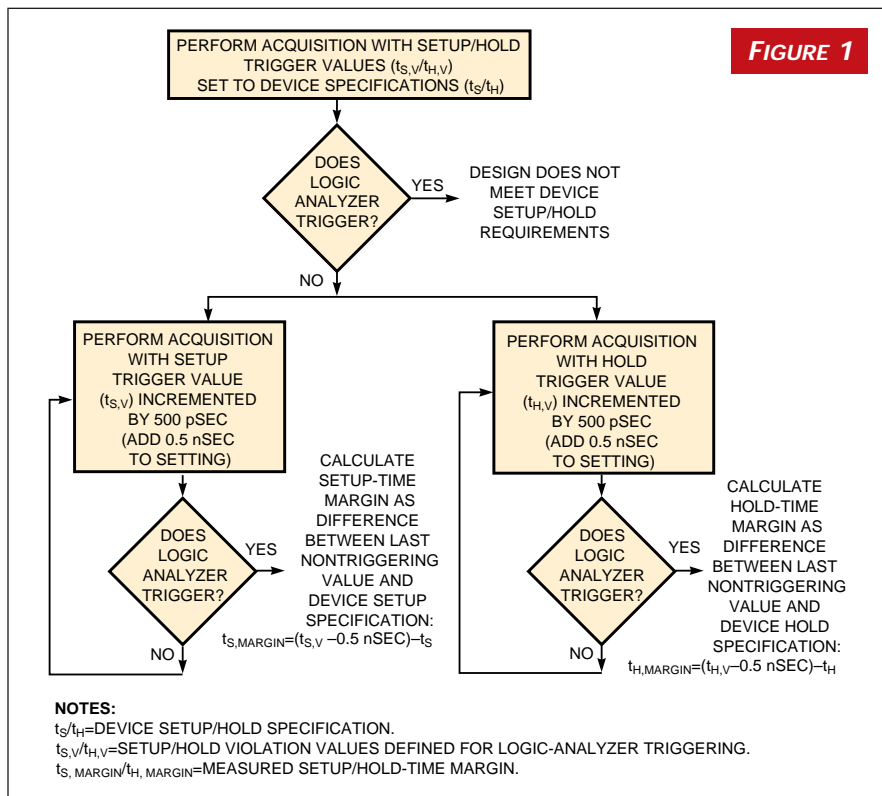
## Increment and measure again

For each successive acquisition, you increment the setup/hold triggering-violation time by 500 psec. At some point, the logic analyzer treats the new time as a fault, even though this new time is not a violation for the RAM device. If the logic analyzer does not trigger, you increase the definition of a violation by 500 psec more and repeat the process until the instrument finally triggers. When the analyzer does trigger, the timing margin is at least as large as the difference between the last defined value that didn't cause a trigger and the RAM specification indicated in *Figure 1*'s equations.

*Table 1* gives an example of the steps you might follow to measure timing margin using logic-analyzer setup/hold triggering. If the logic analyzer were to first trigger with a setup violation value of 5 nsec, the setup-time margin would be at least (5 nsec–0.5 nsec)–3.5 nsec=1

nsec. Note that (5 nsec–0.5 nsec) represents the last setup value for which the logic analyzer did not trigger (4.5 nsec), so this value is the greatest setup value always satisfied. In this example, 4.5 nsec of actual setup time exceed the RAM setup specification of 3.5 nsec by 1 nsec, so the setup-time margin is at least 1 nsec.

During the setup-time-margin measurement, the defined hold-time violation value remains at 1.5 nsec. In this example, 1.5 nsec is the RAM hold-time specification, which presumably is never violated. (You would already have verified this specification with the logic analyzer, as the first row of *Table 1* indicates.) By leaving the hold-time violation at this value, you know that setup time must be the cause of triggers that occur when you increase the defined logic-analyzer violation. You would use a similar technique to measure hold-time margin: Define the logic-analyzer setup violation at 3.5 nsec (the RAM-setup-time specification), and increase the defined hold-time violation beyond the 1.5-nsec RAM specification.



Using logic-analyzer setup/hold triggering, follow this procedure to characterize setup/hold timing margins with 500-psec resolution.

**TABLE 1-LOGIC-ANALYZER SETUP/HOLD-TRIGGER VIOLATION VALUES**

Setup ( $t_{s,v}$ ) (nsec)	Hold ( $t_{h,v}$ ) (nsec)	Does logic analyzer trigger?	Timing-margin observation
3.5	1.5	No	Design meets device specifications.
4	1.5	No	Setup-time margin $t_{s,margin}$ $4 \text{ nsec} - 3.5 \text{ nsec} = 0.5 \text{ nsec}$ .
4.5	1.5	No	Setup-time margin $t_{s,margin}$ $4.5 \text{ nsec} - 3.5 \text{ nsec} = 1 \text{ nsec}$ .
5	1.5	Yes	Setup-time margin $t_{s,margin} < 1.5 \text{ nsec}$ $t_{s,margin}$ $(5 \text{ nsec} - 0.5 \text{ nsec}) - 3.5 \text{ nsec} = 1 \text{ nsec}$ .
3.5	2	No	Hold-time margin $t_{h,margin}$ $2 \text{ nsec} - 1.5 \text{ nsec} = 0.5 \text{ nsec}$ .
3.5	2.5	Yes	Hold-time margin $t_{h,margin} < 1 \text{ nsec}$ $t_{h,margin}$ $(2.5 \text{ nsec} - 0.5 \text{ nsec}) - 1.5 \text{ nsec} = 0.5 \text{ nsec}$ .

Note: This sample procedure measures setup-time margin greater than 1 nsec and hold-time margin greater than 0.5 nsec on a data bus connected to RAM devices that have a 3.5-nsec/1.5-nsec setup/hold specification.

## TIMING-MARGIN MEASUREMENT

A logic analyzer with setup/hold triggering not only lets you measure timing margins, but also provides the productivity you need to rigorously perform complex timing characterization without compromising time to market. Unlike an oscilloscope, with which you manually measure individual signals' setup/hold times, a logic analyzer can simultaneously measure large numbers of setup/hold times with much greater automation. Whereas time-to-market pressure might prohibit exhaustive oscilloscope measurements of all signals' timing margins, the automated logic-analyzer approach permits simultaneously measuring an entire bus.

Furthermore, a logic analyzer can characterize setup/hold under realistic operating conditions over extended periods. Unlike an oscilloscope, a logic analyzer does not depend on a repetitive trigger pattern, so you can use nonrepetitive patterns. You can also search for setup/hold violations by running logic-analyzer acquisitions over nights and weekends. During such acquisitions, you can vary factors, such as temperature, to assess timing margins across the full range of operating conditions. With logic-analyzer setup/hold triggering as a tool, you can significantly increase the rigor of prototype-timing characterization.

### Maximizing design margin

With a logic analyzer that has high-speed timing capability as well as setup/hold triggering, you even have an advantage for maximizing margins. When a logic analyzer triggers on a setup/hold time, a high-resolution timing display can reveal the reason the instrument triggered. You can then use this knowledge of the problem's source to modify the design to improve its margins.

Returning to the memory-subsystem example, suppose that bit 19 of the RAM-data bus has a circuit-board trace that is 500 psec shorter than the other bits. While characterizing hold time, the logic analyzer might first trigger with a hold time of 2.5 nsec, yielding a timing margin of only (2.5 nsec–0.5 nsec)–1.5 nsec=0.5 nsec. The timing display of a logic analyzer that has 500-psec timing could reveal bit 19 as the only RAM-data signal that changes 2 nsec after the RAM-write signal. All other signals might change 2.5 nsec or more after the active write-signal edge.

This scenario indicates that bit 19 is limiting the hold-time margin for the RAM-data bus. If you could increase this signal's delay to match the others—perhaps by lengthening the circuit-board trace length—you could double the hold-time margin.

You can use setup/hold characterization and high-resolution timing analysis to perform a Pareto analysis of signals' timing margins. You can then focus improvement efforts on signals whose timing stands out from the rest until all signals on the bus have roughly equal timing margins. This approach allows you to efficiently attain the maximum margin you can reasonably achieve.

### Key to design confidence

Logic analysis with setup/hold triggering can reveal a design's true timing margin. Despite the large numbers of

high-speed signals in today's digital systems, the ability to simultaneously measure entire buses permits efficient-yet-rigorous characterization. Logic-analyzer timing characterization can instill confidence in a design, provide a thorough understanding of timing margins, and even allow margin optimization without compromising time to market. The extra margin that a logic analyzer enables could prove critical in covering the range of component variation that almost always occurs during a design's production lifetime. **EDN**



### Author's biography

*Colin L. Shepard is a hardware-engineering manager at Tektronix Inc (Beaverton, OR). He has devoted most of his career to logic-analyzer development, in which he has held both project-leadership and design-engineering roles. He earned an MBA from the University of Oregon's (Eugene, OR) Executive Program in 1996, an MSEE from the Massachusetts Institute of Technology (MIT, Cambridge, MA) in 1987, and a BSEE from MIT in 1986. His hobbies include piano, choral singing, and foreign languages.*

### VOTE

Please use the Information Retrieval Service card to rate this article (circle one):

High Interest  
598

Medium Interest  
599

Low Interest  
600