

The future of circuit design

Bill Schweber's editorial, "What's the future of *circuit* design?" (*EDN*, Oct 9, 1997, pg 33), clearly articulates the powerful business forces that are reshaping electronic-system design. Large-scale system ICs have simplified the system-design task to the assem-

bling of standard function blocks, thereby opening the electronic-systems business to intense global competition. Differentiating an electronic-system product has become problematic. Time to innovate is limited because of the increasing pace of new-product introductions from a growing array of global competitors, and the component flexibility that might

enable such innovation is limited with standard large-scale system ICs.

As Schweber asks, "How do you make your product stand out in the crowd if all your competitors have access to the same high-level ICs and chip sets and will be using them in pretty much the same way?" A related question is, "How do I get my new product to market ahead of increasingly nimble competitors who got their first samples of next-generation ICs when I did?"

These fundamental forces drive the burgeoning sales growth of CPLDs and FPGAs. These devices have rapidly grown in capacity to allow some standard functions offered by standard system ICs (standard microcontrollers and bus interfaces, such as PCI and USB) to be incorporated within them along with logic. The designer can customize this logic to create a standout product with significant competitive advantage.

High-density programmable logic also provides relief from intensifying time-to-market pressures via in-system reprogramming (ISR). ISR allows "instant" iteration of a system design and hardware verification by downloading a new design directly to devices installed on a system board. Rapid design iteration and immediate hardware confirmation allow many more design approaches to be tried in less time, resulting in more robust, more innovative designs.

Designers can extend this design flexibility and market responsiveness into finished goods by using ISR capability with a base-system design to implement multiple customer- or application-specific product versions that are configured directly on finished boards on demand, as required by customer-order mix.

High-density programmable logic is returning control of system architecture to the system designer, allowing greater creativity while streamlining the design process. It is an essential tool for every system designer aiming to win in the global systems market.

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UPDATED TABLE 5—FRAME-BUFFER SIZES

Graphics mode	Resolution					Color depth (bits)
	640×480 pixels	800×600 pixels	1024×768 pixels	1280×1024 pixels	1600×1200 pixels	
2-D	300 kbytes	468.8 kbytes	768 kbytes	1.3 Mbytes	1.9 Mbytes	8
	600 kbytes	937.5 kbytes	1.5 Mbytes	2.5 Mbytes	3.7 Mbytes	16
	900 kbytes	1.4 Mbytes	2.3 Mbytes	3.8 Mbytes	5.5 Mbytes	24
	600 kbytes	937.5 kbytes	1.5 Mbytes	2.5 Mbytes	3.7 Mbytes	8
3-D (8-bit Z, 0-bit alpha)	900 kbytes	1.4 Mbytes	2.3 Mbytes	3.8 Mbytes	5.5 Mbytes	16
	1.2 Mbytes	1.9 Mbytes	3 Mbytes	5 Mbytes	7.4 Mbytes	24
	900 kbytes	1.4 Mbytes	2.3 Mbytes	3.8 Mbytes	5.5 Mbytes	8
3-D (8-bit Z, 8-bit alpha)	1.2 Mbytes	1.9 Mbytes	3 Mbytes	5 Mbytes	7.4 Mbytes	16
	1.5 Mbytes	2.3 Mbytes	3.8 Mbytes	6.3 Mbytes	9.2 Mbytes	24
	1.2 Mbytes	1.9 Mbytes	3 Mbytes	5 Mbytes	7.4 Mbytes	8
3-D (16-bit Z, 8-bit alpha)	1.5 Mbytes	2.3 Mbytes	3.8 Mbytes	6.3 Mbytes	9.2 Mbytes	16
	1.8 Mbytes	2.8 Mbytes	4.5 Mbytes	7.5 Mbytes	11 Mbytes	24
	1.5 Mbytes	2.3 Mbytes	3.8 Mbytes	6.3 Mbytes	9.2 Mbytes	8
3-D (24-bit Z, 8-bit alpha)	1.8 Mbytes	2.8 Mbytes	4.5 Mbytes	7.5 Mbytes	11 Mbytes	16
	2.1 Mbytes	3.2 Mbytes	5.3 Mbytes	8.8 Mbytes	12.9 Mbytes	24
	1.8 Mbytes	2.8 Mbytes	4.5 Mbytes	7.5 Mbytes	11 Mbytes	8
3-D (32-bit Z, 8-bit alpha)	2.1 Mbytes	3.2 Mbytes	5.3 Mbytes	8.8 Mbytes	12.9 Mbytes	16
	2.4 Mbytes	3.7 Mbytes	6 Mbytes	10 Mbytes	14.7 Mbytes	24

Corrections and updates

In “Advanced DRAM puts you in the fast lane” (*EDN*, Oct 9, 1997, pg 52), **Table 5** was incorrect. Thanks to Jerzy R Chrzaszcz, PhD, from the Computer Graphics Laboratory at the Institute of Computer Science, Warsaw University of Technology, Poland, for his assistance in correcting this information. The corrected table appears left.

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