

Current limiting defuses the dc/dc time bomb

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ICs' increasing density and speed have caused a proliferation in the number of voltages required to operate electronic subsystems. System designers who use low-voltage ASICs and microprocessors must often design dc/dc power supplies to provide local regulation. When you design a dc/dc converter, you should consider incorporating protection features to improve system reliability. One of the most common protection features is current limiting, which you can implement in a variety of ways.

When you design a current limiter, you need to think about two main areas. First, you must decide how to measure the current. (Table 1 summarizes the techniques.) Second, you must use the measurement results in a circuit that starts to protect at the desired current level. Current-limiter design necessitates trade-offs among cost, complexity, reliability, and performance. Analyzing and comparing the several approaches can help you understand the trade-offs.

The traditional approach is to use a low-ohmic-value current-sense resistor in series with the power-supply output. The voltage across such a resistor is directly proportional to the output current. A differential amplifier compares the voltage across the resistor with a current-trip-point reference. The resistor dissipates power, which lowers the power supply's overall efficiency and adds to the already complex problem of power-system thermal management.

To limit the power dissipation in the current-sense path, you must lower the resistor values as the current levels increase. Recently, resistor manufacturers have made significant progress in producing low-ohmic-value, low-inductance, high-accuracy current-sense resistors. You can find cost-effective surface-mount resistors with resistances as low as 5 m Ω , 2W power ratings, and 1% tolerance. These resistors work in supplies whose output current is as high as 15A. For a little more money, you can use resistors with resistances as low as 1 m Ω . The advances in sense-resistor technology result from the development of alloys that provide stable low resistance over a wide temperature range. For example, temperature coefficients of less than ± 75 ppm/ $^{\circ}\text{C}$ are fairly com-

If components' impedance is all that limits a dc/dc converter's output current, the circuit is a time bomb—waiting to destroy not only itself, but also other parts of your system. There are many ways to sense and limit the current. You must understand them to intelligently choose among them.

mon. An example of a family of high-accuracy, low-ohmic-value sense resistors is Dale's (www.vishay.com/vishay/dale.html) WSR-2 series.

In a buck regulator, you can sense the output current by placing the current-sense resistor in series with the inductor or in series with either MOSFET (Figure 1).

When you put the resistor in series with the inductor (Figure 1a), the output current flows through the resistor. This method provides the best accuracy because it directly measures the output current. In addition, by sensing the average voltage across the resistor, you can sense the average current. Also, you can use a less expensive resistor than you would need with some other approaches, because the resistor need not have especially low parasitic inductance. However, this method dissipates the most power ($P=I_{\text{O}}^2 \times R_{\text{SENSE}}$). Elantec's (www.elantec.com) EL7571C buck-regulator IC uses this output-sensing technique.

Placing the resistor in series with Figure 1b's top FET improves the efficiency because the output current flows through the sense resistor only during the ON time. $P_{\text{D}}=I_{\text{O}}^2 \times R_{\text{SENSE}} \times \text{DC}^{1/2}$, where P_{D} is power dissipation, and DC is duty cycle. A low-inductance resistor is essential because the resistor is in series with the high-current switch. Capacitive discharge and inductive ringing at the sense node require removing artifacts from the voltage that represents the sensed current. Leading-edge blanking in the current-sense amplifier can remove these artifacts. Finally, the sense-resistor voltage reflects only the peak current; the average voltage does not represent the average output current. Maxim's (www.maxim-ic.com) MAX1626 uses top-FET-resistor sensing.

When you place the resistor in series with the bottom FET (or diode in a nonsynchronous buck converter), you also improve efficiency, because the output current flows through the sense resistor only during the off-time (Figure 1c). $P_{\text{D}}=I_{\text{O}}^2 \times R_{\text{SENSE}} \times (1-\text{DC})^{1/2}$. Depending on the converter's duty cycle, this method can offer better efficiency than top-FET-resistor sensing. Bottom- and top-FET-resistor sensing

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have similar limitations. Micro Linear's (www.microlinear.com) ML4900 uses bottom-FET-resistor sensing.

To reduce the power system's cost, you can substitute a pc trace for the current-sense resistor. You should carefully design the trace to handle the output current. First, you must determine the trace width. If the board uses 1-oz copper, allow a trace width of 20 mils for every ampere of output current. Once you determine the trace width, calculate the sense-resistor value as follows:

$$R_{\text{TRACE}} = \rho \times \text{LENGTH} / \text{WIDTH} \times \text{THICKNESS},$$

where ρ is the resistivity of copper, which is $1.673 \times 10^{-8} \Omega\text{m}$ at 25°C . The thickness of 1-oz copper is about 1.3 mils (33 μm). For first-order analysis, the following formula determines the trace length:

$$\text{LENGTH} \approx 40 \times I_{\text{O}} \times R_{\text{SENSE}}$$

where I_{O} equals output current in amperes, R_{SENSE} is in milliohms, length is in mils, and the trace width is 20 mils/A. For example, a 5-m Ω trace that can support 10A of output current must be 200 mils wide and 2 in. long. Such a trace may be impractical where board area is at a premium.

To obtain practical resistor values, the trace must usually be fairly long. Such a trace has inherently high parasitic inductance and requires significant board area. These characteristics limit the use of the pc-board-trace-sense technique to the application in **Figure 1(a)**, where the resistor is in series with the inductor. When you use a pc-board trace as a sense resistor, the resistor disappears as a separate component, but its power dissipation remains, and the system design must account for it.

The biggest disadvantage of pc-board-trace sensing is the sense element's poor overall accuracy. Variations in pc-board

fabrication and raw-material properties cause the trace impedance to vary significantly. To minimize the variation, you can route the trace on an inner layer, which eliminates plating as an error source. However, although an inner-layer trace is more accurate, it suffers from poor heat transfer. You must consider heat transfer when you determine the maximum current density.

In practice, you can achieve $\pm 20\%$ room-temperature resistance accuracy, but, because copper exhibits a 4000-ppm/ $^\circ\text{C}$ temperature coefficient, the sense-resistor value changes by 40% from 0 to 100°C . Furthermore, you should expect large temperature swings in a power supply whose traces carry high currents. Fortunately, increased current increases the resistance, reducing the current-limit trip point at elevated temperatures and eliminating the possibility of thermal runaway.

The overall accuracy of the pc-board-trace-sense technique is about -40% . Despite this poor accuracy, some manufacturers recommend using the pc-board trace to reduce cost. Cherry Semiconductor (www.cherry-semi.com) does so in its CS5166 data sheet.

FET switches can sense current

One FET characteristic that you can use for current limiting is the switch's on-resistance. Most FET data sheets specify this resistance, $R_{\text{DS(ON)}}$. Because this technique can sample the current only during the FET's on-time, the measurement timing can be complex and can require high-speed circuits in the control IC. However, because the power supply already uses the FETs for switching, FET sensing adds little cost and imposes no efficiency penalty.

Before it samples the current, the current-limit circuit should allow time for transients to settle after the FET turns on. This blanking period, together with the propagation delay of the current-sense circuit, determines the FET's min-

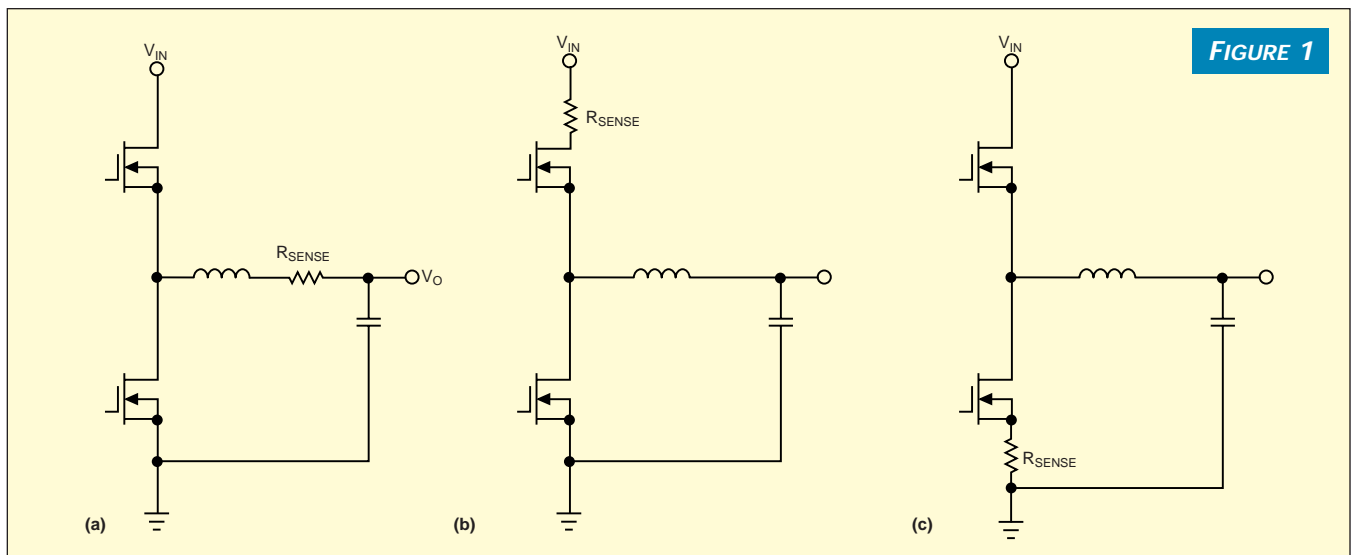


FIGURE 1

You can place a current-sensing resistor in several locations in a dc/dc converter's output stage. The most obvious place is in series with the inductor of the output L-C filter (a). A sense resistor in series with the drain of the top MOSFET dissipates less power (b). You can also place the resistor in series with the source of the bottom MOSFET (c). Here, the resistor carries current only when the load is receiving energy from the inductor's magnetic field.

imum on-time. At a given frequency, this minimum on-time translates into a minimum duty cycle. Under short-circuit conditions, a buck regulator with a constant-current-limiting scheme reduces its duty cycle to an extremely low value in an attempt to limit the output current. Delays in the current-limiting circuit increase the short-circuit duty cycle and produce current runaway because of volt-second imbalance. Linear Technology's (www.linear-tech.com) LTC1430 provides an example of top-MOSFET current sensing.

To avoid current runaway, you can sense the current across the bottom FET, as does Micro Linear's ML4902. However, if you use the bottom FET, you can't control peak currents or use pulse-by-pulse current limiting. These limitations exist because the current sensing takes place during the off-time, which is out of phase with the cause of the overcurrent condition. To work properly, a bottom-FET-sense circuit should analyze several cycles before it initiates current limiting.

The resistance's initial tolerance and temperature coefficient affect the accuracy of the current-sense information that the FET provides. Moreover, vendors' parts behave differently from each other. Typically, the ON resistance of a given type of FET varies by $\pm 20\%$ from sample to sample. Vendor variations can cause an additional $\pm 10\%$ variation. Circuit operating conditions, such as gate-to-source voltage and drain current, account for another $\pm 15\%$ variation. Finally, the FET's temperature coefficient of resistance is about 5000 ppm/ $^{\circ}\text{C}$, causing a $\pm 25\%$ variation from 0 to 100 $^{\circ}\text{C}$. The total of these variations is $\pm 70\%$ from the nominal value, which is equivalent to a maximum-to-minimum ratio of 5.67-to-1. As with the pc-board-trace technique, the FET's temperature coefficient is positive, so that the current appears greater at elevated temperatures, preventing current runaway.

Low output voltage means high current

An intriguing technique that provides low cost, improved efficiency, and high peak currents is output-voltage monitoring. This technique takes advantage of the fact that the output voltage drops significantly under short-circuit conditions. By sensing a drastic reduction in output voltage, this approach lets you initiate protective action. Because the power supply already senses the output voltage, most of the necessary circuitry is already inside the control IC. During start-up, the power supply's output capacitors behave as a short circuit. Therefore, this technique requires a time-out circuit to disable protection during start-up.

Like MOSFET sensing, output-voltage monitoring requires no additional current-sense element, allowing the highest possible efficiency and lowest cost. Output-voltage sensing uses the inherent impedance of the power path—from the unregulated supply through the MOSFET, the inductor, and the pc-board power plane—to effectively sense a severe overcurrent condition. In most cases, the dominant failure mode is a short circuit in the load, which output-voltage monitoring detects well enough.

Because this method senses the output voltage, it is ideal for use in systems in which peak currents are much higher than the average current. Examples of such systems are today's high-speed microprocessors, which generally operate at 60% of their specified maximum current rating. By using output-voltage sensing, you can achieve improved efficiency, lower cost, and design simplicity. Cherry Semiconductor's CS5165, a regulator for Intel's (www.intel.com) Pentium II μP , uses output-voltage sensing.

Transformers sense ac current

Another popular technique for sensing current is to use a current-sensing transformer. This method is expensive, large, somewhat difficult to implement, and limited to ac information. However, transformers offer several advantages, such as isolation, level shifting, and high efficiency.

The transformer's unique advantage is that it can provide an isolated current-sensing signal to the controller. This feature allows direct sensing of the secondary current in an isolated system. The isolated current signal is also useful in applications that require high-side current sensing. This need usually arises because of the current-sense amplifier's limited common-mode-voltage range. Control ICs, such as the industry-standard 3842, provide no differential current-sensing capability. A current-sensing transformer allows circuits based on such ICs to offer this capability.

Another advantage of transformer current sensing is that it allows you to design a transformer to provide any desired signal level. Typically, the primary side of the current-sensing transformer has just one turn. By defining an appropriate turns ratio and termination resistor, you can set the sensing voltage to virtually any level.

Transformer sensing has advantages and disadvantages. A transformer can provide only ac-current information, which does not allow an accurate measurement of average current. Designing with a current-sensing transformer is common yet difficult. You must optimize the turns ratio, determine the termination-resistor value, consider the low- and high-

TABLE 1—A COMPARISON OF CURRENT-SENSING TECHNIQUES

Current-sense technique	Accuracy	Cost	Power dissipation	System-design complexity
Resistor	$\pm 5\%$	\$0.25	High	Medium
PC-board trace	$\pm 50\%$	None	High	Medium-to-high
MOSFET	$\pm 70\%$	None	None	Medium
Output voltage	NA	None	None	Low
Transformer	$\pm 10\%$	\$0.40	Low	High

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frequency response, and account for the transformer's leakage inductance. Sense transformers are also large and relatively expensive.

When it obtains the current value, the limiting circuit compares the current with a threshold level and initiates protection if the current reaches a hazardous value. There are several ways to restrict the load current. **Table 2** compares various approaches. Before you examine these techniques, note that any current-sensing technique can work with virtually any current-limiting technique.

The controller can average the current-sensing information over several cycles to improve the accuracy of the output-current measurement and to enhance noise immunity. It is also common to use the current-sensing information directly to provide pulse-by-pulse current limiting, which provides the fastest shutdown and thus the best protection.

In constant-current limiting, when the output current reaches the preset limit, the control loop reduces the duty cycle to maintain the maximum allowable current (**Figure 2a**). The output voltage drops to a value determined by the product of load impedance and the fixed output current. The regulator delivers the full output current into a short circuit. To keep the inductor in volt-second balance (that is, to keep it from saturating), the power supply's duty cycle dramatically drops. Because of the output-voltage characteristic, this current-limit approach is often called a "brick-wall" current limit.

Because an overcurrent situation reduces the output voltage only proportionally, a constant-current limit can be advantageous in circuits that drive dynamic loads. You might choose this type of limiting for its simplicity, particularly in a current-mode control system, which inherently provides constant-current limiting. Additionally, this technique ensures a constant switching frequency for any load condition, including overcurrent.

The main problem with the brick-wall current limit is that it delivers the full output current into the load during an overload condition. The high current can cause catastrophic system failures. Moreover, the regulator acts as an energy

source to fuel the destruction of the load. Additionally, the high current levels, which can continue for long periods, can seriously reduce the power supply's reliability. During a fault, some supply components dissipate more power and some dissipate less power than they do during normal operation. For example, during a short circuit in a buck regulator, the bottom FET (or catch diode) takes most of the stress away from the top FET. To avoid failure, you must oversize the bottom FET for the sole purpose of handling short circuits. To survive sustained short circuits, a regulator that uses brick-wall limiting needs larger, more costly components and a larger, more costly pc board than it needs for normal operation. Raytheon's (www.raytheon.com) RC5050 series employs brick-wall current limiting.

Foldback current limiting

In a variation on constant-current limiting, foldback limiting reduces, or folds back, the output current in response to an overcurrent condition. A foldback current limiter senses the output voltage and, at lower output voltages, either proportionally lowers the current-limit threshold (**Figure 2b**) or reduces the current in one step.

The main purpose of the foldback feature is to limit the shift of power dissipation within the regulator during current limiting. The lower short-circuit current reduces the overall power dissipation and improves reliability. As does the constant-current technique, this method provides constant-frequency operation over the full current range. Like constant-current limiting, foldback limiting is advantageous in supplies that drive dynamic loads.

The greatest obstacle to implementing foldback is powering up with a heavy load. When the power supply attempts to start up into a full load, the output may never reach the nominal voltage. Thus, the supply may never deliver its full output voltage. The power supply can "latch" in the foldback state and cannot start up until an operator removes the load. To avoid this problem, the system designer must characterize the load at power-up and set the minimum foldback current above the maximum start-up current. Although

TABLE 2—A COMPARISON OF CURRENT LIMITING IN BUCK-CONTROLLER ICs

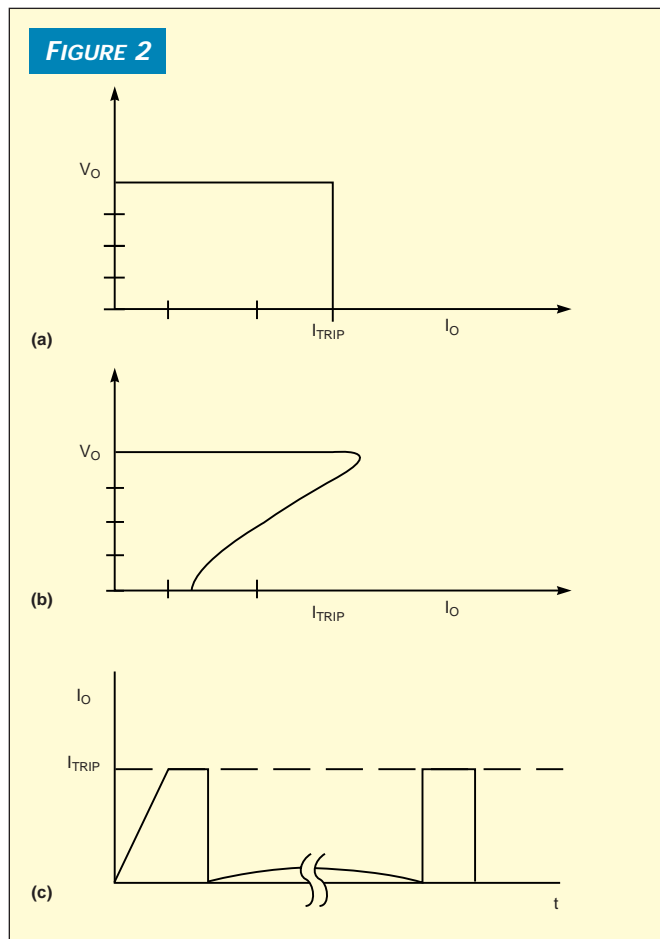
Part no.	Manufacturer	Control method	Sense technique	Current-limit approach
3842	Industry standard	Current mode	Current-sense transformer	Constant-current limit
CS5165	Cherry Semiconductor	V2	Output-voltage sense	Hiccup short-circuit protection
CS5166	Cherry Semiconductor	V2	Resistor or pc trace	Hiccup current limit
EL7571C	Elantec	Current mode	Resistor or pc trace	Constant-current limit
LT1430	Linear Technology	Voltage mode	Top MOSFET	Constant-current limit
MAX1626	Maxim	Pulse-frequency modulation	Resistor in series with top FET	Constant-current limit
ML4902	Micro Linear	Voltage mode	Bottom FET or resistor in series with bottom FET	Hiccup current limit
RC5050	Raytheon	Current mode	Resistor or pc trace	Constant-current limit
TL5001	Texas Instruments	Voltage mode	Output-voltage sense	Overcurrent shutdown
UC3830	Unitrode	Current mode	Resistor or pc trace	Foldback current limit

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foldback improves the power supply's reliability, it does not necessarily provide additional protection for the load, because the power supply can deliver moderate currents to the load. Unitrode's (www.unitrode.com) UCC3830 uses foldback limiting.

In overcurrent shutdown, when the current reaches the limit trip point, the controller simply shuts off the power supply. Typically, restarting the supply requires cycling the input power off and then on again. To avoid accidental turnoff under start-up and other dynamic conditions, add a delay between the detection circuit and the shutdown event.

This technique provides the safest approach, because the power turns off, and there is no possibility of thermal stress. Additionally, this method is simple and cost-effective to implement. The ac/dc power supplies in PCs use this approach.



Brick-wall limiting delivers the same current to a short circuit as it does to a normal load (a). During a fault, the power supply's components must dissipate much of the power that would normally go to the load. Foldback limiting reduces the output current under short-circuit conditions but can cause latch-up during power-up (b). Hiccup limiting, one form of which appears in (c), cuts back the output current during fault conditions but repeatedly attempts to restart normal operation.

The primary drawback to overcurrent shutdown is the need to cycle the input power to restore operation. However, the need to cycle power can alert an operator to the fact that a fault occurred and thus can enable the operator to investigate the need for corrective action. Texas Instruments' (www.ti.com) TL5001 uses overcurrent shutdown.

Hiccup current limiting incorporates overcurrent shutdown but adds an automatic-restart mechanism. The power supply shuts down for a time and automatically restarts when the time-out expires (Figure 2c). As in overcurrent shutdown, the shutdown delay determines the power supply's on-time during a short circuit. To reduce power dissipation, minimize the ratio of the power-on time to the shutdown time.

Hiccup current limiting can achieve low power dissipation and low component stress under overload conditions. The automatic-restart feature reduces the need for servicing and maximizes system availability. Automatic restart is important when the input voltage powers multiple systems or subsystems, and power cycling would cause an outage in a portion of the system that is unrelated to the fault.

Hiccup current limiting adds some complexity to start-up timing, shutdown, and automatic-restart. However, power-control ICs, such as Cherry Semiconductor's CS5155, simplify the design of power supplies with hiccup limiting.

To determine the best approach, you should consider the suitability of the current-limiting techniques to your system's application. Sometimes, the best choice is a combination of approaches. For example, you might use constant-current limiting for an initial period and initiate hiccup limiting if the fault persists. Table 2 compares the overcurrent-protection features of modern power-control ICs. EDN

Authors' biographies



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