

# Supervisory circuit monitors modem connection

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In telemetry or security applications in which a modem connection automatically establishes itself between two systems, a failure in one of the systems can interrupt the data exchange while the connection remains established until someone physically breaks the line or restarts the failed system. This situation can also happen if your PC crashes during a long-lasting Internet download. To prevent this problem, the circuit in **Figure 1** continuously supervises the RS-232C data lines (TxD and RxD) and automatically hangs up the connection when the circuit detects a long period without transmitted or received data.

The TxD and RxD inputs to the circuit (pins 2 and 3 on the D-type RS-232C connector) first drive line receiver  $IC_1$ , whose outputs then drive the two inputs of  $IC_2$ 's dual retriggerable monostable multivibrator (one shot). When the system establishes a new connection, the first exchange of data triggers  $IC_2$ , and positive pulses of duration  $T_X = 0.45 \times R_X \times C_X$  appear at the 1Q and 2Q outputs. Each new transition on the

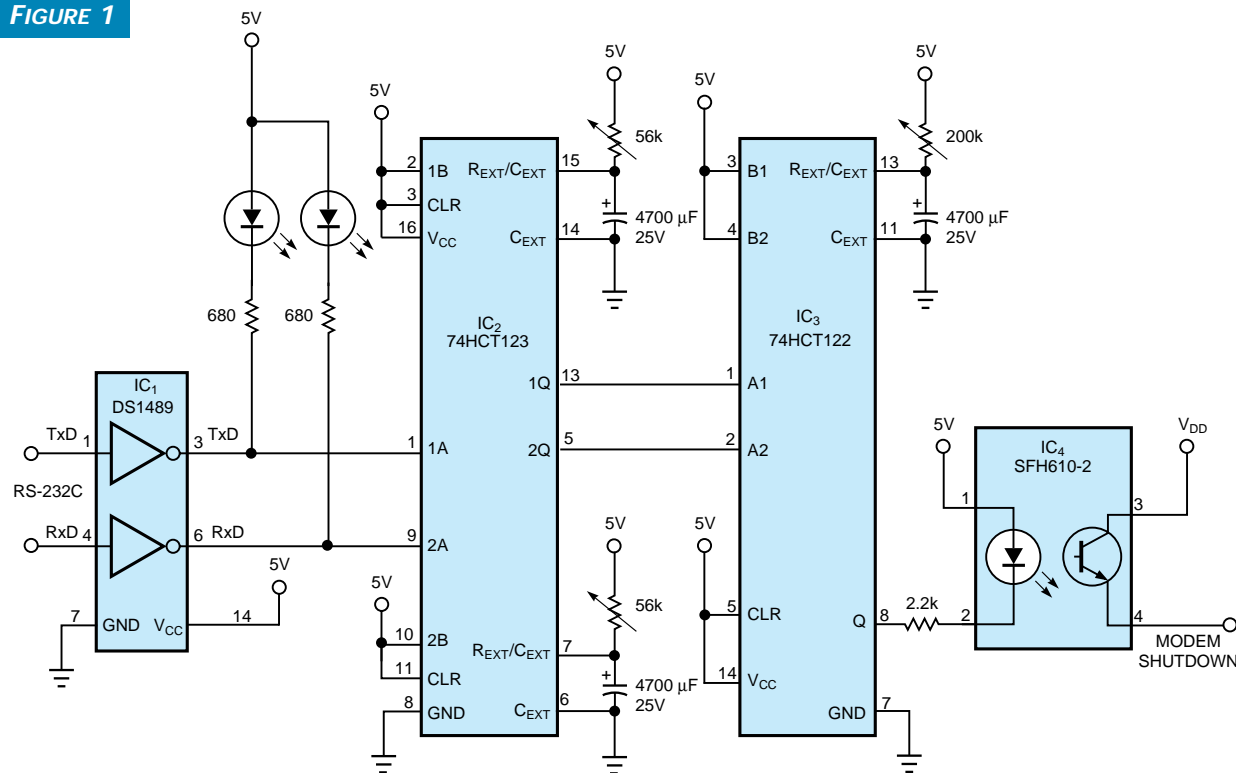
data lines retriggers the associated one shot, which extends the output pulse for a new period,  $T_X$ . In this application,  $R_X = 56 \text{ k}\Omega$ , and  $C_X = 4700 \text{ }\mu\text{F}$  corresponds to a period of about 2 minutes.

If a problem arises with one of the systems and it stops transmitting data for a period longer than  $T_X$ , the corresponding one shot's output pulse goes low, indicating that the system should hang up the connection. To allow for the self-restarting of the system, another one shot,  $IC_3$ , shuts down the modem for a period  $T_Y$ , determined by the associated timing resistor and capacitor.

The conditioning circuit for the output signal uses an optocoupler,  $IC_4$ , to drive the shutdown input of the modem. If your modem has no shutdown input, you can solve the problem by powering the modem through a relay driven by  $IC_4$ . (DI #2186) EDN

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FIGURE 1



A lack of activity on the TxD or RxD lines fails to retrigger  $IC_2$ , which causes the circuit to hang up the modem connection.

# Circuit optimizes phototransistor bandwidth

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A simple circuit can improve the dynamic performance of a phototransistor for use in low- to medium-speed applications as fast as 100 kbps, such as optical isolation of an RS-232C serial line (Figure 1). In low-cost applications that require high voltage insulation, low part count, and low power, you can use consumer components, such as Siemens' SFH421 IR LED with an SFH320 IR phototransistor. The rise/fall-time rating of the LED is 500 nsec, which is fast enough, but the phototransistor's rise/fall time is 5  $\mu$ sec for the fastest version and 8  $\mu$ sec for the slowest with a 1-k $\Omega$  load.

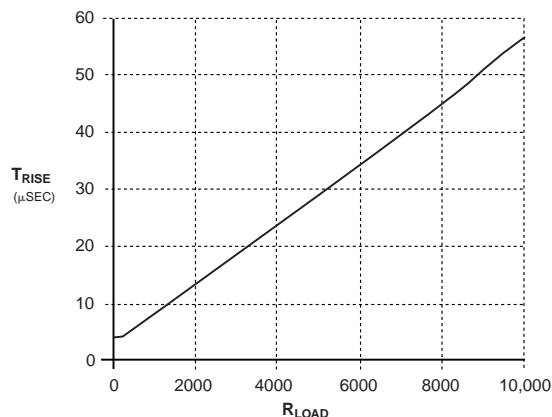
Phototransistors have less favorable dynamic behavior than do photodiodes because, in addition to the collecting and charging processes, phototransistors also experience a delay stemming from the amplification mechanism (Miller effect). For the rise and fall time of a phototransistor, the following relationship applies:

$$t_{r,f} = \sqrt{(1/2f_T)^2 + b(R_{LOAD} \cdot C_{CB} \cdot V)^2},$$

where  $f_T$  is the transition frequency,  $C_{CB}$  is the collector-base capacitance,  $V$  is the gain, and  $b$  is a constant whose value lies between 4 and 5. For  $R_{LOAD}=1$  k $\Omega$ ,  $4 < b < 5$ ,  $100 < V < 1000$ ,  $C_{CB} \approx 2.5$  pF, and  $f_T \approx 100$  kHz, the result is  $5 \mu\text{sec} < t_{r,f} < 8 \mu\text{sec}$ .

A plot of rise time vs load resistance provides a more practical way to evaluate the maximum transmission speed of Figure 1a's circuit without using additional compensation circuitry (Figure 2). For a 2400 bps serial link with less than

FIGURE 2

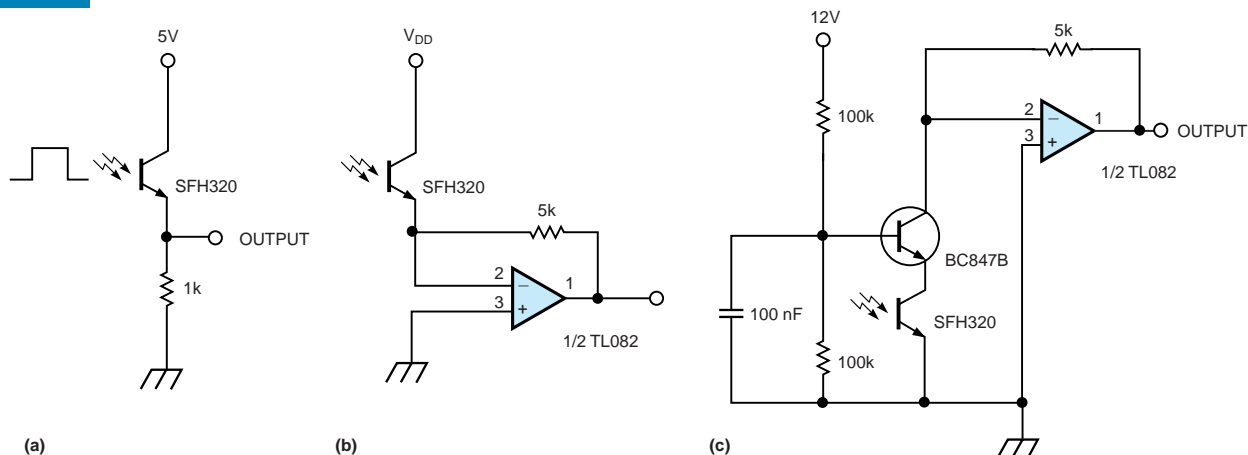


The relationship between worst-case rise time and load resistance for the basic phototransistor circuit indicates that for a  $t_{RISE}$  of 42  $\mu$ sec,  $R_{LOAD}$  should equal 7.5 k $\Omega$ .

10% error on the bit length, the rise-time estimate is 42  $\mu$ sec, which corresponds to a 7.5-k $\Omega$  resistor.

To get a faster response time, you can use an op amp, but

FIGURE 1



A basic phototransistor (a) has a 5- to 8- $\mu$ sec rise/fall time with a 1-k $\Omega$  resistor. An op amp can improve a phototransistor's response time (b) but performs poorly without additional phase compensation. Alternatively, you can use a transistor to isolate the phototransistor's capacitance and to hold the signal voltage across the phototransistor to a stable dc value (c).

without phase compensation the result is poor. In **Figure 1b**'s circuit, the phototransistor's internal capacitance and the amplifier's gain bandwidth limit the overall speed. To cancel the side effect of the phototransistor's  $C_{CB}$ , the amplifier needs a small capacitor in parallel with  $R$ . Choosing the right value for the compensation capacitor is a difficult task, because the current-to-voltage converter exhibits a two-pole response. Also, to ensure stability, you need to consider phase compensation and bandwidth together.

Fortunately, there is another way to get the best of the phototransistor bandwidth. You can isolate the phototransistor's internal capacitance with a transistor (**Figure 1c**). The

transistor, with its low output impedance and its large gain bandwidth, holds the signal voltage across the phototransistor to a stable dc value. The versatile BC847 can do the job, and, with Siemens' SFH320, the circuit can reach a transmission speed of 153.6 kbps. You can't increase the speed beyond this point, even with the fastest op amp, because of the photoelectric delay that the charging and collecting processes cause. (DI #2188) EDN

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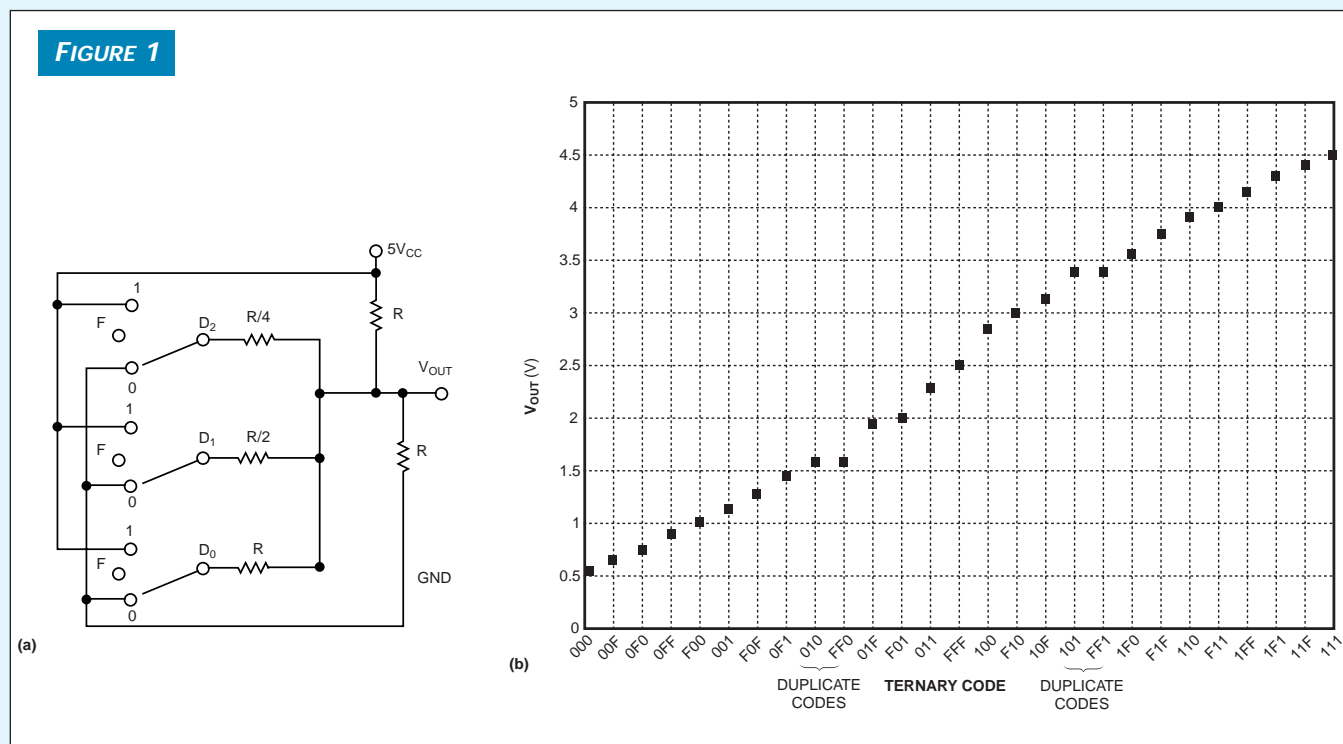
## Technique increases low-cost DAC's resolution

JEREMY DEAN, THOMSON-THORN MISSILE ELECTRONICS LTD, BASINGSTOKE, UK

Cost-sensitive  $\mu\text{C}$  applications often employ resistor chains to implement crude DACs. You can extend this method by exploiting the way in which many  $\mu\text{C}$ s allow individual output pins to be set to either low ("0"), high ("1"), or floating ("F") states. A converter can thus respond to ternary rather than binary codes.

The resistive network in **Figure 1a** has three inputs. Allow-

ing each input to be either 0, 1, or F results in the transfer characteristic in **Figure 1b**. Allowing for two duplicate cases results in 25 distinct output levels. Thus, the technique achieves roughly  $4\frac{1}{2}$  bits of resolution while using only three pins of a  $\mu\text{C}$  and five resistive elements. The transfer characteristic is symmetrical about midrail and does not extend to the supply rails, making it inherently suitable for use in



Providing three possible inputs—1, 0, and F (floating)—to the resistor network (a) produces a ternary-code transfer characteristic (b).

single-supply applications. Note that the characteristic is nonlinear, which shouldn't matter for many applications.

A practical circuit implementation uses a single-inline array to form the resistive network (Figure 2). The PIC16C84 (Microchip Technology, [www.microchip.com](http://www.microchip.com)) code in Listing 1 uses a look-up table to convert binary inputs to the required ternary outputs. (You can download this listing and the related look-up table from EDN's Web site, [www.ednmag.com](http://www.ednmag.com). At the registered-user area, go into the

Software Center to download the file from [DI-SIG, #2189](#).)

You can expand or contract this ternary technique with-in reason. For example, using four  $\mu\text{C}$  pins gives 75 distinct output levels, and even just two  $\mu\text{C}$  pins gives seven levels. By saving pins, the technique is ideally suited for use with the PIC12C50X family, which has very limited I/O in an eight-pin package. (DI #2189) EDN

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### LISTING 1—PIC16C84 DAC CODE

```

; Title: c:\edn\cheapdac\code_v1.asm
; Author: Jes Dean
; Dated: 20/10/97
; Function: Program continually loops, reading 5 bit binary i/p
;          from RB4-0, and outputting ternary codes on RA2-0
;          suitable for driving resistor array as demonstrator.

LIST P=16C84

PC      equ 0x02 ; Relevant system registers...
STATUS equ 0x03
PORTA   equ 0x05
PORTB   equ 0x06
TRISA   equ 0x85

temp    equ 0x10 ; Temporary storage.

org 0x00
goto main

org 0x10
; For brevity, no explicit initialisation done. PORTA, PORTB initialise
; as inputs with no weak pull-ups, and all interrupts are disabled.
main    movf PORTB,0 ; Read PORTB
        movwf temp ; and store.

        sublw 26
        btfsc STATUS,0 ; IF 0-<w<26
        goto inrange ; THEN temp is in correct range.
        movlw 26
        movwf temp ; ELSE
        ; Limit temp to 26.

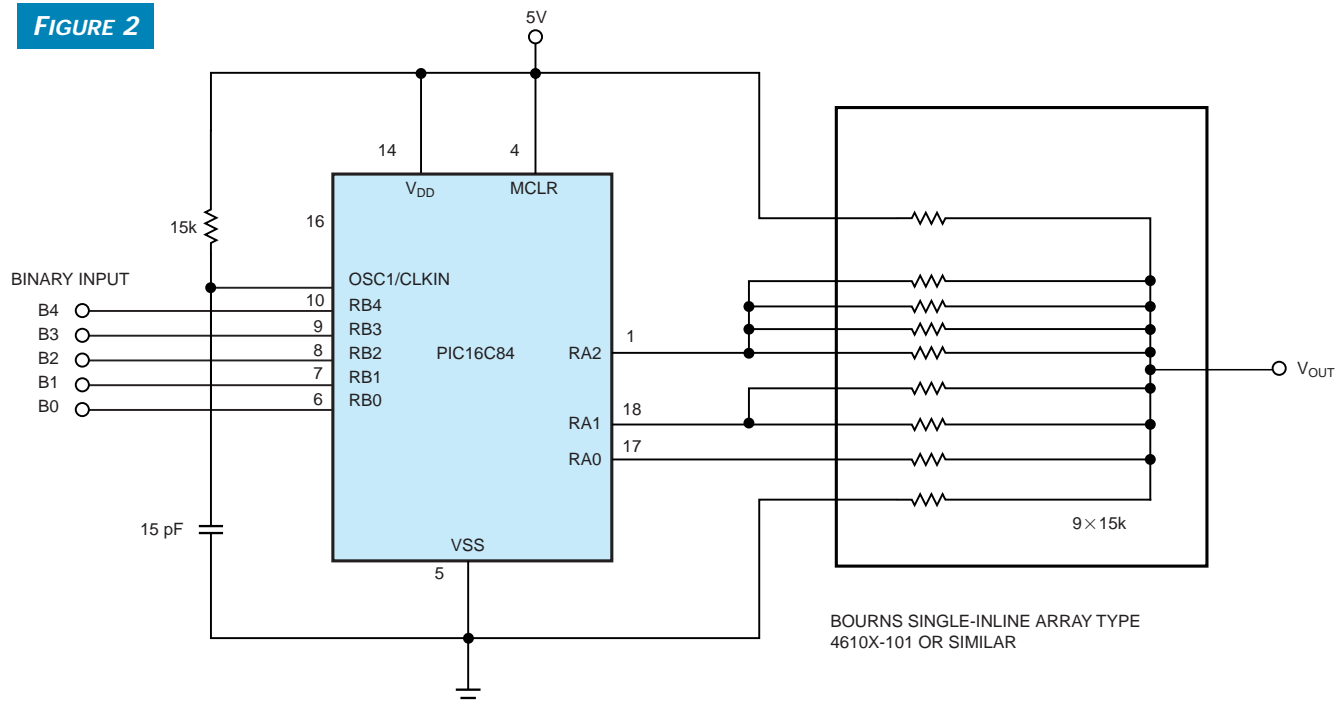
inrange movf temp,0 ; Copy temp to w
        call ra_lut ; and call look up table.
        bsf STATUS,5 ; Enable addressing of TRISA (in Bank 1)
        movwf TRISA ; Set RA2-0 as inputs or outputs accordingly.
        ; (Note RA4,3 will be set spuriously.)
        bcf STATUS,5 ; Disable addressing of TRISA (in Bank 1)
        movwf temp
        swapf temp,0
        movwf PORTA ; Put relevant data on pins set as outputs.
        ; (Note RA4,3 may be set spuriously.)

        movlw 0xff ; Delay loop to allow value to
        movwf temp ; settle for measurement purposes.
loop1   decfsz temp,1
        goto loop1

        goto main ; Repeat eternally.

```

FIGURE 2



A simple DAC demonstration circuit comprises a PIC16C84  $\mu\text{C}$  and a single-inline-resistor array.

# Undersampling extends utility of digital scopes

ROBERT J INKOL, DEFENCE RESEARCH ESTABLISHMENT, OTTAWA, ON, CANADA

By undersampling the input signal, you can use a digital oscilloscope to digitize and display or collect signal data of even RF and IF signals. To sample a signal without aliasing, you must use a sampling rate that satisfies the relationship

$$f_M = f_S/2$$

where  $f_M$  is the maximum allowable signal frequency and  $f_S$  is the sampling rate. If you want the sampled signal data to directly form a high-quality visual representation of the signal waveform, a considerably higher sampling rate is necessary. A practical implication of this equation for high-frequency signals is that you can acquire sequences of signal data for only short periods before the available memory is filled.

However, many high-frequency signals, such as RF and IF signals in communications systems, are bandpass signals whose bandwidths are very small relative to the center frequencies. Consequently, you can intentionally undersample these signals so that their spectral components alias to lower frequencies. To ensure that the spectral

$$f_L \geq mf_S,$$

components of the signal do not fold over on themselves or become reversed, you must choose the sampling rate,  $f_S$ ,

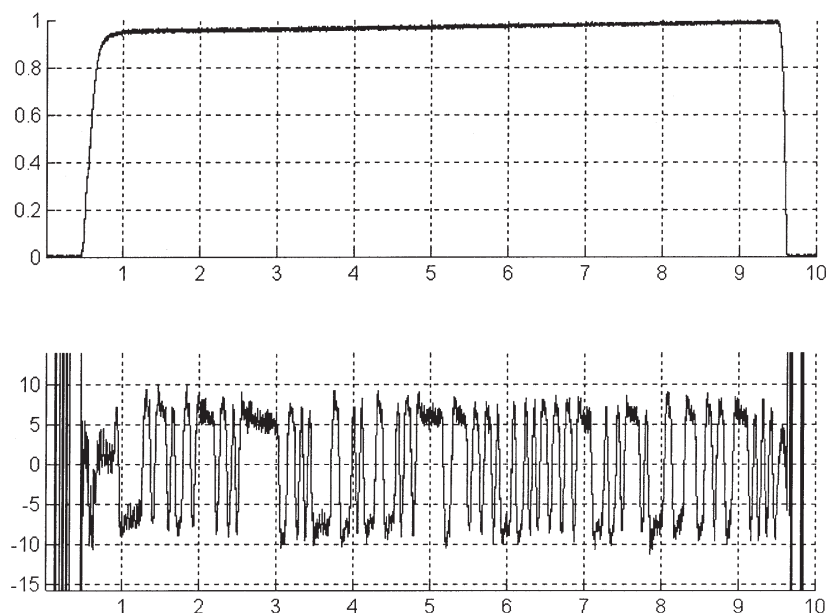
$$f_U < (2m+1)f_S/2,$$

such that simultaneous solutions exist for and

where  $m=f_L/f_S$  (an integer) and  $f_L$  and  $f_U$  are the respective upper and lower bounds for the bandwidth that the signal of interest occupies. The undersampled signal differs from the original signal by a downward shift in frequency of  $mf_S$ . In carrying out this concept, you need to disable analog low-pass filters at the oscilloscope input or ensure that the filters have a cutoff frequency high enough to preserve the signal information.

You can apply this concept to practical applications, such as the digitization, storage, and analysis of the RF-signal output from a VHF radio that employs frequency-hopping techniques. In this application, the radio was programmed so

FIGURE 1



An undersampling technique helps capture the envelope (a) and instantaneous frequency (b) of a single hop from a typical frequency-hopping radio using FSK modulation.

that the signal would hop to a carrier frequency of 71.9 MHz at frequent intervals. A bandpass filter centered about 70 MHz with a bandwidth of 5.6 MHz attenuated and band-limited the transmitted signal. A LeCroy ([www.lecroy.com](http://www.lecroy.com)) 9354 digital sampling oscilloscope, operating at a sampling rate of 10 MHz, generates records of 100k data samples. The choice of carrier frequency and sampling rate results in the aliasing of the RF signal to 1.9 MHz. Note that the use of a sampling rate of 200 or 250 MHz would not allow the storage of sufficient data for a complete hop.

You can then use Mathworks' ([www.mathworks.com](http://www.mathworks.com)) Matlab to implement signal-processing algorithms for amplitude and frequency demodulation of data sequences associated with individual hops. **Figure 1** shows the time-domain behavior of the amplitude and instantaneous frequency measured for a representative hop signal. You can discern the FSK modulation in the switching of the instantaneous frequency between two discrete frequencies. (DI #2190) EDN

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selection and gain control. The format is simple: The system must first pull the Load line on the LM1973 low and then pulse 16 clocks on the Clock line with a corresponding 16 bits of input data on the Data-in line. The 16 bits of data comprise 8 address bits, which select one of the three channels and 8 attenuation bits, which select the attenuation setting for the selected channel. This data format is most significant bit first with the address bits first and the attenuation bits immediately after. This straightforward format could be difficult to implement in a prototype without a controller, but the BSII makes a “kluge” programmer devilishly simple.

This example uses only one channel of the LM1973, although using all three channels is just as simple. Two normally open pushbuttons—one for up and one for down—provide an active high when depressed (Figure 1). You also need to connect the following three BSII outputs to the digital potentiometer: I/O 8 to Data (Pin 11 for LM1973), I/O 9 to Clock (Pin 9 of LM1973), and I/O 10 to Load (Pin 10 of LM1973)

The meat of the code required for this application comprises two BSII instructions: Button and Shiftout. Button

checks the status of a BSII input line and allows for branching according to that status. This example monitors the up and down buttons until one is pressed and then reprograms the LM1973 accordingly. The Shiftout instruction shifts out a data word synchronously along with a clock output. You select the appropriate output pins and specify a most-significant-bit-first protocol, as the LM1973 demands.

This minimal code provides up/down programming on a single channel but is easily expandable to provide other functions, including data readback from the serial device, multiple channels, or custom programming sequences. You can easily edit the code on the PC, debug the code with the BSII connected to the PC, and then download the code and carry it away on the BSII.

Listing 1 is available for downloading from EDN's Web site, [www.ednmag.com](http://www.ednmag.com). At the registered-user area, go to the Software Center to download the file from DI-SIG #2178. (DI #2178)

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## 10-kHz VFC uses charge-pump variation

STEPHEN WOODWARD, UNIVERSITY OF NORTH CAROLINA, CHAPEL HILL, NC

A diode-capacitor charge pump is the starting point for many voltage-to-frequency-converter (VFC) designs. The circuit in Figure 1 uses a variation on that classic theme to achieve linearity less than 0.05%, micropower operation of approximately 10- $\mu$ A total draw from a 5 to 36V rail, and bipolar-input capability. The basis for these features is the switchable-polarity, self-compensating charge pump comprising  $D_1$  to  $D_4$ ,  $C_1$  to  $C_4$ , and CMOS switches  $S_2$  and  $S_3$ . Although simple in concept, VFCs using diode-capacitor pumps suffer from the need to cope with the nonideal characteristics of diodes used as analog switches.

Temperature-dependent forward-voltage drop, junction and stray capacitance, and reverse leakage current all conspire to limit converter accuracy. The stray capacitance and leakage current are especially troublesome in low-power applications, in which the need to minimize pump-current consumption limits the size of the pump capacitors. Because the total amount of charge pumped in each converter cycle is minimal, the error sources are proportionally more significant and thus harder to control and compensate. The unique pump circuit in this converter comprises two distinct halves:  $D_1$ ,  $D_2$ ,  $C_1$ , and  $C_2$  generate a frequency-proportional current that closes the VFC's feedback loop, and  $D_3$ ,  $D_4$ ,  $C_3$ , and  $C_4$  generate an error-correcting compensation current.

If you assume that  $C_2=C_3=C_4$  and equality of diode for-

ward drops ( $V_D$ ) and stray capacitance ( $C_S$ ), then the net feedback current from the pump is

$$\begin{aligned} f_{\text{OUT}}(2C_1 + C_S) & \left[ 4.55\text{V} \times \frac{2C_1}{2C_1 + C_S} - 2V_D - (4.55\text{V} \times \frac{C_1}{2C_1 + C_S} - 2V_D) \right] \\ & = f_{\text{OUT}}(2C_1 + C_S) \left[ 4.55\text{V} \times \frac{2C_1 - C_1}{2C_1 + C_S} + 2V_D - 2V_D \right] \\ & = f_{\text{OUT}} \times 4.55 \times C_1 = f_{\text{OUT}} \times 10^{-4} \mu\text{A}/\text{Hz}. \end{aligned}$$

You not only obtain compensation for the bothersome  $V_D$ s, but also eliminate the effects of stray capacitance in the bargain. Operation of the converter depends on integrator  $IC_1$ 's control of multivibrator  $IC_3$ . The combination is such that  $f_{\text{OUT}}=0$  when  $IC_1$ 's output is 1.2V. If, for example,  $V_{\text{IN}}>0\text{V}$ ,  $IC_1$  ramps negative. As  $IC_1$  ramps through approximately 0.8V,  $Q_1$  begins to conduct, thereby turning on both  $Q_2$  and  $Q_3$ .  $Q_2$  drives  $S_1$  to the “plus” polarity state, providing a status signal to the connected system (typically, a gated up/down counter). The status signal indicates the presence of a positive  $V_{\text{IN}}$ .  $S_1$  sets up  $S_2$  and  $S_3$  to provide a negative feedback current to  $C_5$ . Subsequently,  $Q_3$ 's collector current causes  $IC_3$ 's  $f_{\text{OUT}}$  to increase until  $1\text{E}-7 \times f_{\text{OUT}} = V_{\text{IN}}/R_1 = 4 \text{ kHz}/\text{V}$



# Single IC biases LCD and GaAsFET amplifier

JOHN WETTROTH, MAXIM INTEGRATED PRODUCTS, APEX, NC

Operating from a lithium-ion cell or a four-cell NiCd battery, the circuit in **Figure 1** provides  $-6V$  bias for LCDs and a separate, quiet negative bias for a GaAsFET power amplifier. This bias combination exists in cell phones, two-way pagers, wireless modems, and many other wireless devices. Not long ago, when most GaAsFET amplifiers required a positive voltage of  $6V$  or more, you could easily obtain the LCD bias by simply inverting the power-amplifier voltage. With the advent of lower voltage power amplifiers and single Li-ion supplies, a negative doubler became necessary for the LCD bias. The various bias-generation techniques in use are generally bulky and require multiple ICs. One alternative is to select an LCD with lower negative bias voltage, but that approach compromises the LCD's temperature performance, contrast, and cost in favor of a simpler bias supply.

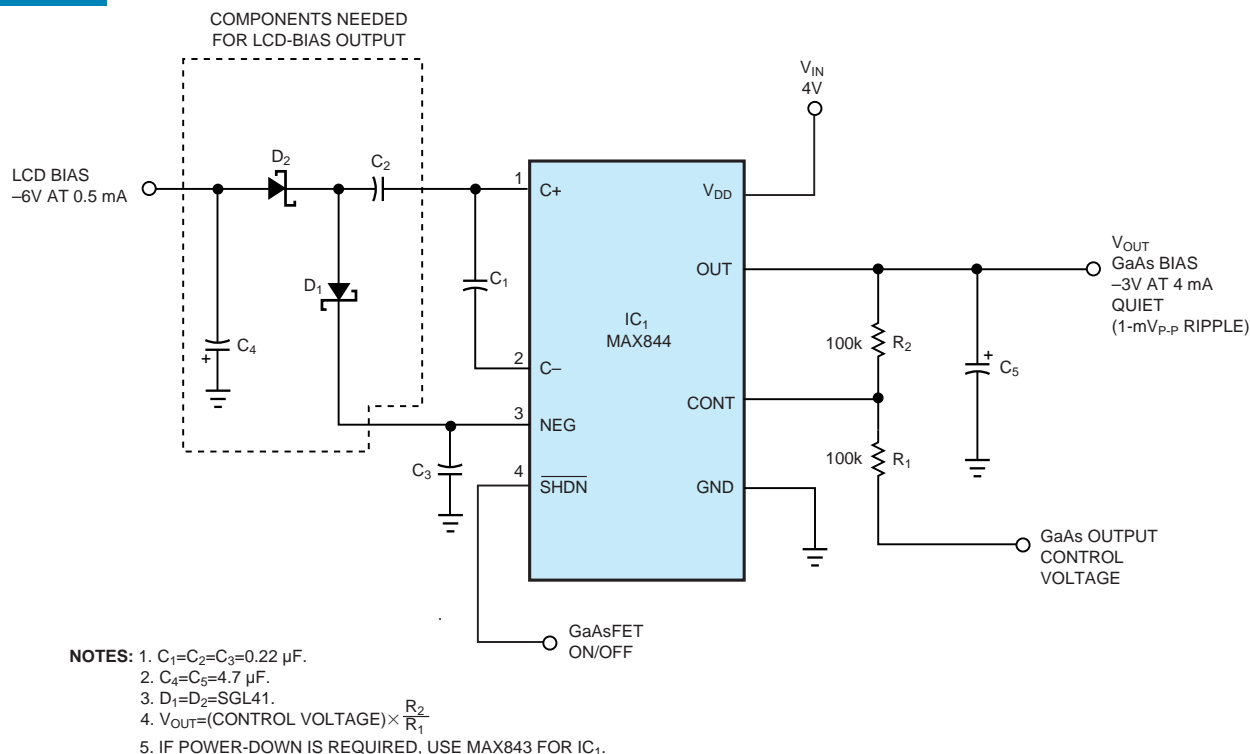
For most systems, the approach is to use two ICs: a negative doubling inverter, such as the MAX865, which provides a negative LCD bias of approximately  $-6V$ , and a linear regulator to provide the  $-3V$  GaAsFET bias. However, even two

ICs can pose a problem in tiny systems. Moreover, a simple linear regulator may generate too much noise, and noise in the GaAsFET bias can appear in the transmitted RF signal. IC<sub>1</sub>, which includes a charge-pump inverter and a low-noise linear regulator in an SO-8 package, generates a quiet GaAsFET bias by design. It operates from supplies as low as  $2.5V$  and produces a negative bias voltage with only  $1\text{ mV}$  p-p ripple. You can change the bias level by adjusting  $R_1$  and  $R_2$ , according to instructions in the data sheet.

Circuitry in the dashed line provides the  $-6V$  LCD bias. A square-wave signal from the charge pump (Pin 1) adds to the unregulated negative voltage at Pin 3 to form a negative, doubled version of the input voltage. The voltage loss (two diode drops) is minimal because of the LCD's low bias current and the use of low-drop Schottky diodes. The diodes drop approximately  $0.2V$ ; a Li-ion cell can thus produce an LCD bias greater than  $-6V$ . (DI #2179) EDN

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FIGURE 1



A charge-pump/linear-regulator IC produces two negative bias voltages for wireless applications.

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