How it works

How copper-topped silicon creates FASTER, LONGER-LASTING CHIPS

By using copper instead of aluminum for an IC's interconnect layers, chip makers can build devices that run faster and use less power. But there's more to the new copper technology than simply replacing one metal with another.

JIM LIPMAN, TECHNICAL EDITOR

It isn't the switching transistors in ICs that limit chips' speeds these days. In ICs fabricated with deep-submicron processes, the connections between transistors add more delay than the transistors themselves—as much as 80% or more of total on-chip delay time. Even though these interconnections are very short and fabricated with aluminum—which, like most metals, has extremely low resistance—the delays are still significant. Solution? Replace a near-zero resistance with an even nearer-to-zero resistance. In short, replace aluminum interconnect with copper.

Except that it's not that simple. And that's too bad, because the ability to place thin layers of aluminum on a piece of silicon to create tiny interconnect wires has been a cornerstone of IC processing for many years. It would be very convenient simply to deposit copper layers in place of aluminum. Unfortunately, copper creates new problems even as it solves old ones, and these new problems require solutions of their own. To understand the complexities, and to fully appreciate the advances in copper technology by companies such as IBM, Motorola, and Texas Instruments, take a look at what's involved in IC interconnect.

Resistance is the key

As advances in CMOS processing technology shrink chip-feature dimensions, both transistors and chip-interconnect wiring get smaller. Metal-interconnect lines affect speed (via RC delays) by their intrinsic resistance and their capacitance, both to ground and to other interconnect lines. To complicate matters, changes in IC fabrication that alter interconnect resistance can also alter capacitance.

The resistance, R, of an interconnect line segment is: $R=\rho\times L\div A$, where ρ is the resistivity of the line, L is the segment length, and A is the cross section of the segment (width times height). The shrinking of dimensions via process improvements places transistors closer together, reducing interconnect length and thus reducing resistance. However, it also results in smaller line widths, thus increasing resistance by reducing cross-sectional area. Increasing line thickness could counteract this increase in resistance, but chip-processing-yield considerations limit metal-interconnect thickness; halving a line's width does not allow doubling its thickness to keep unit-length resistance constant. Thus, as process technologies shrink dimensions, resistance increases per unit length.

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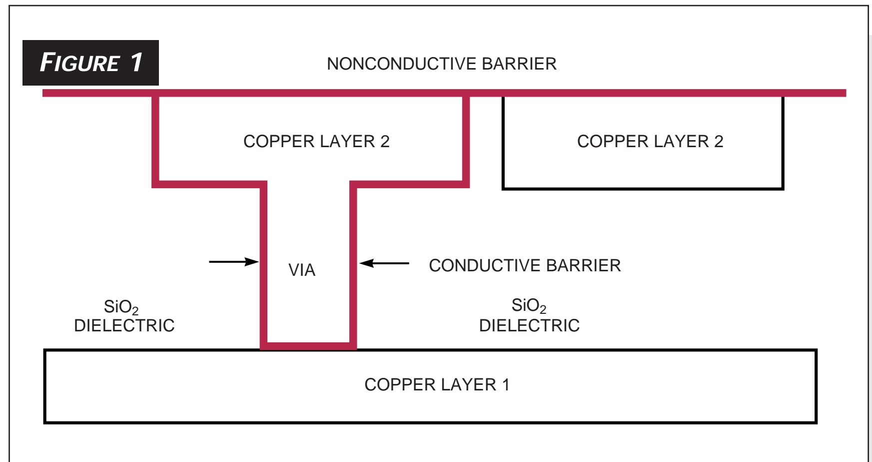
A seemingly obvious solution to this problem is to replace aluminum with copper, which has lower resistivity. At room temperature, pure aluminum's resistivity is 2.8 μΩ-cm, and pure copper's is 1.7 μΩ-cm (**Reference 1**). You can't compare those numbers directly, however, because most semiconductor processes don't use pure aluminum or pure copper as an interconnect material. Process engineers add small amounts of other metals (often copper) to aluminum to im-prove reliability; they add other exotic metals to copper as a shield to keep the copper from contaminating an IC's silicon. The added metals increase the resistance of both aluminum and copper lines, but the resistivity of the copper lines is still around 30 to 40% lower than for aluminum-alloy lines.

Copper's lower resistivity also leads, indirectly, to a capacitance advantage. For a given metal-interconnect pitch (line width plus line spacing), keeping the resistance low means making the lines as thick as process-yield requirements allow. Unfortunately, any speed gained by such a resistance decrease is offset by an increase of side-wall capacitance (the capacitance between adjacent metal lines). This extra sidewall capacitance causes increased coupling and crosstalk between lines, degrading chip performance. By using copper in place of aluminum, however, chip makers can trade off crosstalk capacitance and line resistivity. For identical line dimensions, copper and aluminum provide the same side-wall capacitance, but copper has lower resistance. Similarly, for copper and aluminum lines with equivalent resistance, copper lines can be thinner, resulting in lower side-wall capacitance.



A conductive barrier below copper interconnect lines prevents silicon contamination. A nonconductive barrier above the metal layer prevents undesirable copper oxidation.

Keeping the silicon pure

Copper doesn't provide the proverbial free lunch, though—its advantages are offset by disadvantages. For one thing, copper's mobility in silicon is a problem. Copper atoms can diffuse from the interconnect layer through the SiO_2 dielectric and contaminate the silicon lattice (**Figure 1**). To work as a semiconductor, a silicon substrate must be pure, with extremely low levels of accurately measured impurities that give the substrate its desired characteristics. Copper contamination alters the very properties that make silicon a good semiconductor.

Companies isolate copper from a silicon substrate by depositing a barrier layer between the copper and the dielectric layer. This barrier not only prevents the copper from diffusing through the insulating layer into the silicon substrate, but also helps the copper adhere to the SiO_2 dielectric.

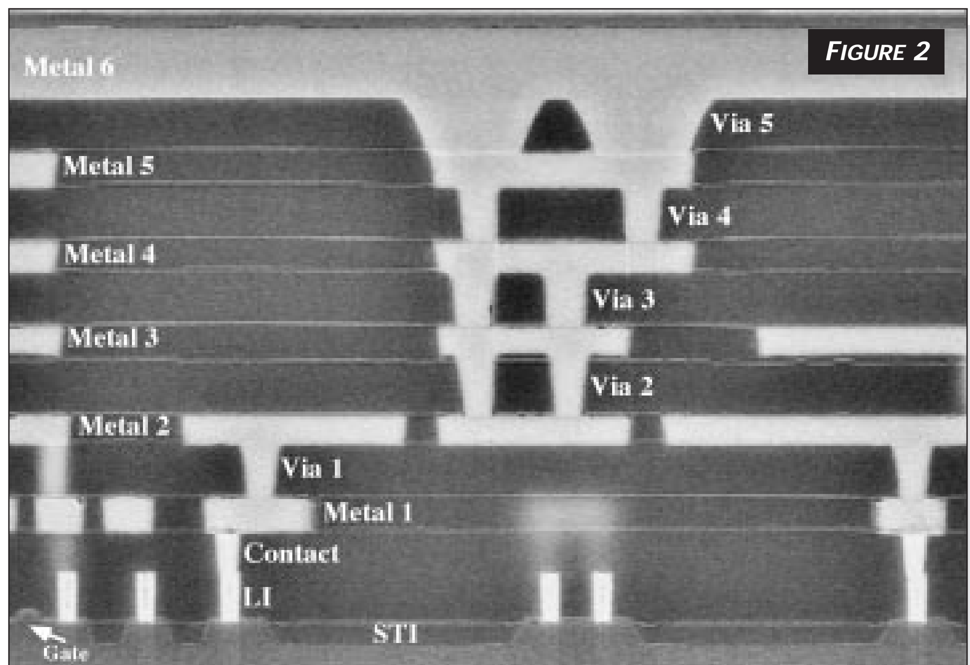
Copper's oxidation characteristics introduce another problem. Unlike aluminum, in which initial oxidation forms a protective layer that prevents further oxidation, copper can oxidize indefinitely. In time, this oxidation can make copper interconnects unreliable. The solution in **Figure 1** is a nonconductive barrier over the copper. Normal chip processing includes a passivation layer of insulating material on top of a chip. This passivation layer helps keep moisture away from the chip's surface but is not airtight. The nonconductive barrier on top of a copper-interconnect layer forms a hermetic seal and thus keeps oxidation to a minimum.

Better reliability

With copper's problems overcome, its advantages—increased reliability with high current, for example—come to the forefront. Over time, high current in a metal interconnect causes the metal to deteriorate at the location where current density is highest—the place with the smallest cross section. As current forces metal atoms to move away from that location and in the direction of the current flow, the situation worsens: the cross section decreases further, current density increases, and, eventually, the line opens. This phenomenon, "electromigration," is a reliability-limiting problem for silicon chips. Copper has a higher electromigration threshold than aluminum, however, meaning that chips with copper interconnects have a higher reliability than do chips that use aluminum with the same inter-

connect cross-section dimensions.

Another reliability advantage of copper over alumi-num results from copper's lower resistivity. Lower resistance for a given interconnect length and cross section means less heat dissipation at a given operating voltage. For high-current lines, such as power grids, the power decrease can be significant, resulting not only in longer chip life but also in better chip performance. In addition, copper has higher thermal conductivity than aluminum. The higher con- ductivity allows the copper to conduct more heat away from the silicon die, where it degrades logic speed, and to carry it to the package for more efficient dissipation.



Motorola's dual-inlaid copper processing reduces chip-process steps and results in a planar surface, increasing chip yield.

The use of copper can also eliminate some of the process steps in chip fabrication, thereby reducing cost. Most modern, conventional chip processes use two conductors—aluminum for connectivity between transistors on the same layer and tungsten in the vias, or conductive paths, between metal layers. A copper process reduces fabrication complexity by using copper for both metal traces and vias.

Figure 2 shows a typical sequence of steps in copper-technology implementation. The first step is the etching of a via into the SiO_2 insulating layer. A second etch step defines the metal lines. A conducting barrier metal then lines the chip to prevent copper from diffusing through the insulator into the silicon and to help the copper adhere to the SiO_2. The next step deposits copper on the chip. Finally, a chemical-mechanical planarization (CMP) step removes excess copper and barrier material. The CMP step leaves copper in only the desired chip areas and results in a flat, or planar, surface, which is necessary for subsequent high-yield metal-deposition layers. Both IBM (www.chips.ibm.com) and Motorola (www.mot.com/sps/general) have demonstrated chips with six layers of copper interconnect.

Reducing delays even more

Still not content with copper's significant boosts in chip speed, some companies are working to reduce interconnect delays even further. As previously mentioned, substituting copper interconnect for aluminum primarily speeds chip operation by decreasing line resistance and thus decreasing RC delays. To further reduce RC delays, semiconductor companies, such as NEC (www. nec.com) and Texas Instruments (www.ti.com), are trying to reduce capacitance by experimenting with insulating materials other than SiO_2 between copper layers.

Capacitance between metal layers in a chip scales directly with the dielectric constant of the insulator between the layers. SiO_2 has a dielectric constant of 3.9. Companies are investigating other "low-k" materials, including different forms of silicon-oxygen compounds (SiO_x) and other insulators with dielectric constants in the range of 1.3 to 3.0. Use of these materials in production-semiconductor processing will have to wait, however. Silicon foundries still have to solve problems such as dielectric adhesion to silicon, long-term stability, and the matching of the dielectric thermal coefficient of expansion of the insulator to that of silicon.

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You can reach Technical Editor Jim Lipman at 1-925-606-1370, fax 1-925-606-1563, ednlipman@mcimail.com.