

EDN LEADING EDGE

WHAT'S HOT IN THE DESIGN COMMUNITY

EDITED BY FRAN GRANVILLE

Converter lets PCs use Firewire to talk to IEEE 488 instruments

The IEEE 1394 Firewire bus may be the wave of the future, but the IEEE 488 general-purpose instrumentation bus isn't going away any time soon (see "Despite threats from USB and Firewire, IEEE 488 ain't down yet," pg 67). However, the trend toward "sealed" PCs makes it harder to use IEEE 488 interface cards that reside within the PC. That's where bridge products come in. These units connect to external ports on the PC and enable communication with instruments' via buses, such as the ubiquitous IEEE 488. Such bridge products must provide software transparency, which allows test programs to control instruments as if the instrument were connected to an ISA- or PCI-bus-based IEEE 488 interface.

National Instruments, which offers Universal Serial Bus (USB)- and Ethernet-to-IEEE 488 bridge units, is now introducing a unit that uses the IEEE 1394 Firewire serial bus to perform a similar function. Firewire offers a 400-Mbps maximum burst-transfer rate. That speed is 50 times as great as that of IEEE 488 itself and almost 100 times as fast as any



Your PC can communicate with IEEE 488 instruments via Ethernet, USB, or using the new GPIB-1394 converter (right foreground) via the IEEE 1394 Firewire high-speed serial bus.

device can communicate via USB. The \$695 GPIB-1394 receives power from the Firewire bus and can communicate over the bus at 400, 200, or 100 Mbps. The unit implements the full range of normal and extended IEEE 488 talker and listener functions, including serial and parallel

polling, service requests, and pass/receive control functions.

—by Dan Strassberg

National Instruments, Austin, TX. 1-800-258-7022, fax 1-512-683-8411, info@natinst.com, www.natinst.com. **Circle No. 424**

Bring in 'da noise; bring in 'da filter

Filtering to eliminate undesired inband or out-of-band noise is a standard design requirement, and the MSU1HFx family of switched-capacitor IC filters from Mixed Signal Integration can simplify your task. You configure these universal filter ICs using resistors for lowpass, highpass, elliptic, bandpass, notch, or allpass modes using external resistors. The resulting design requires zero to nine resistors, depending on filter type and response. You can set corner or center frequencies as high as 500 kHz, select nominal clock-to-corner frequency ratios of 6.25-to-1 or 12.5-to-1,

and obtain attenuations as high as 40 dB.

Two of the eight-pin devices save power by operating at frequencies as high as 100 kHz, typically requiring 5 mA from a 5V supply; the 500-kHz versions draw 20 mA. You can also choose a 16-pin version that contains two filter sections, or you can cascade the single-section filter ICs for higher order functions. Prices begin at \$3.75 (1000).—by Bill Schweber

Mixed Signal Integration, San Jose, CA. 1-408-434-6305, fax 1-408-434-6417, www.mix-sig.com.

Circle No. 425

Monolithic cascode amplifier fulfills cascade of RF needs

Because of their reverse-isolation potential, cascode-transistor amplifiers work well as RF functional blocks, such as VCOs, buffers, low-noise amplifiers, and mixers. Two

with a 2.7V supply, although it can operate from a 5V supply. It also offers 44-dB reverse isolation at that frequency. Maximum bias current is 5.6 mA; the on-chip bias circuitry yields better temperature stability than you could achieve with external bias circuitry. Output power for this IC is 2.3 dBm at 1-dB gain compression, also at 850 MHz; for maximum application flexibility, you provide the matching circuitry outside the IC.

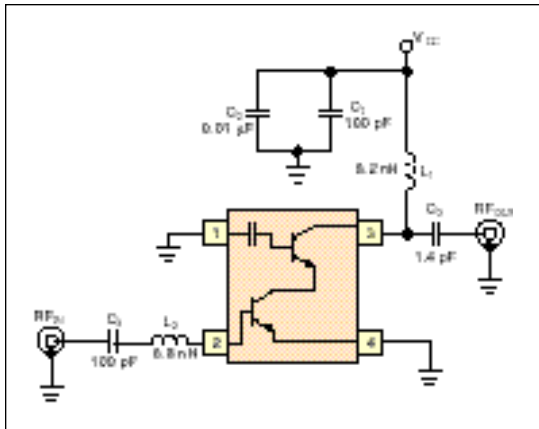
The similar MRFIC0915 operates at 2.5-mA maximum bias current, thus saving power, but consequently has reduced isolation performance of 38 dB. The devices' data sheets list scattering parameters for each 100-MHz point in their operating range, easing modeling and design.

The MRFIC0915 and 0916 cost \$0.75 and \$0.90, respectively (10,000).

—by Bill Schweber

Motorola Semiconductor Products Sector, Phoenix, AZ. 602-413-4991; fax: 1-602-413-7986, www.motorola.com/wireless-semi.

Circle No. 426



Using the internally biased MRFIC0916 cascode-transistor amplifier, you can build an 850-MHz amplifier that yields typical 18.5-dB gain and 44-dB reverse isolation from a 2.7V supply.

related cascode devices from Motorola for 100-MHz to 2.5-GHz operation save board space by integrating all requisite bias circuitry and by using a four-pin SOT-143 surface-mount package. The MRFIC-0916 provides 18.5-dB typical and 20.5-dB maximum gain at 850 MHz

REACH US VIA E-MAIL

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Single chip switches for the whole Ethernet family

Texas Instruments' new ThunderSwitch II for Giga and Fast Ethernet and ThunderSwitch I for 10-Mbps desktop switches support IEEE standards for full- or half-duplex operation on all ports, virtual-LAN interoperability, and packet priority levels. The products also provide link aggregation, or "trunking," to combine multiple ports into one logical channel. The switch chips collect Etherstat (Ethernet Statistics, a subset of simple-network-management-protocol management-interface bases) and remote-monitoring statistics on a per-port basis to reduce the work of the switch-management CPU.

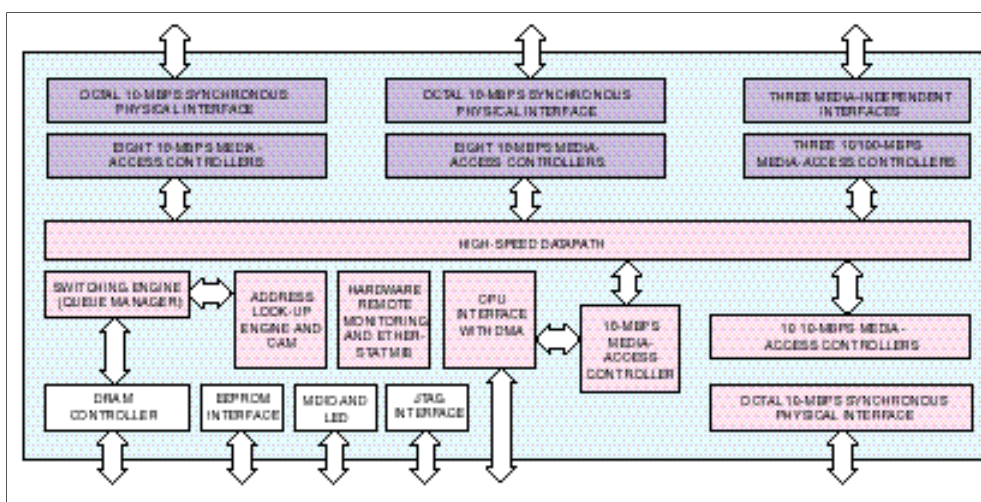
The first chip in the ThunderSwitch II family, the TNETX4090, offers eight 10/100-Mbps ports and one 100-Mbps/1-Gbps uplink port. This device uses Rambus DRAM (RDRAM) to get 4-Gbps memory bandwidth from a memory chip. In addition, you can use the Giga Ethernet uplink port to cascade as many as four TNETX4090s to design a 32-port Fast Ethernet switch. Alternatively, for switches with more ports, you can use a "port-awareness" mode on the device and an additional stand-alone crossbar switching device. Samples of the TNETX4090 are available in 352-bump

BGA packages and cost \$90 (10,000).

The ThunderSwitch I family incorporates four pin-compatible devices. Using the same package for all four devices provides a pc-board design that supports four port densities. The devices use a core that operates at 2.5V. All four devices have three 10/100-Mbps uplink ports. The \$95 (10,000) TNETX3270 offers 24 10-Mbps ports, the \$85 (10,000) TNETX3190 has 16 10-Mbps ports, the \$76 TNETX3151 has 12 10-Mbps ports, and the \$55 TNETX3110 has eight 10-Mbps ports.—by Stephen Kempainen

Texas Instruments, Dallas, TX. 1-800-477-8924, ext 4500, www.ti.com/sc/.

Circle No. 427



The 24-port, single-chip switch ThunderSwitch TNETX3270 offers a high level of functional integration.

DSL yields very high-speed Internet access

Digital-subscriber-loop (DSL) technology spawned chip and reference-design announcements from Rockwell and Broadcom at the recent Supercomm show in Atlanta. Rockwell Semiconductor introduced chip sets for both asymmetrical-DSL (ADSL) remote modems and central-office applications. Meanwhile, Broadcom promoted a reference design for very high-speed DSL (VDSL) that incorporates the BCM6010 DSL transceiver chip.

Rockwell's entry into the ADSL market offers chips for both ends of twisted-pair telephone cabling. Both the remote modem and the central-

office chip sets use the Falcon discrete-multitone (DMT) transceiver technology from a joint development with Pairgain Technologies (www.pairgain.com), a DSL modem company. The V.90/ADSL Combo chip set for remote-access modems employs a multitasking architecture for concurrent legacy analog and ADSL-modem operations. The three-chip set dissipates less than 2W and provides functions for either the 56-kbps V.90 analog-modem standard or the full-rate, 8-Mbps ANSI T1.413 Issue 2 ADSL standard. You can program the chip set for upgrades to support the International Telecommunication

Union's emerging G.lite standard for the 1.50-Mbps-bit-rate, low-cost consumer version of ADSL that aims to eliminate splitters at remote sites. The Combo chip set's sampling will coincide with the expected finalization of the G.lite standard in the fourth quarter of this year. The chip set costs \$67.50 (10,000).

The central-office ADSL modem chip set from Rockwell supports eight ports, useful for adding native ADSL to central-office switches and remote digital-loop carriers. The chip set limits dissipation to 1.9 and 2.7W per channel, respectively, for G.lite and full-rate modes. The chip set uses a

low-power RISC controller to manage eight ADSL line transceivers and a single-chip asynchronous-transfer-mode (ATM) Utopia Level II physical-layer device. Samples of the Octal G.lite/ADSL device set will be available in the fourth quarter and will cost \$67.50 (10,000) per port.

Attacking the VDSL market, Broadcom introduced the BCM96011 reference design for a modem that operates at 25.92 Mbps when using twisted-pair telephone cable as long as 3500 ft. You can configure the modem to support either remote- or central-office applications. The reference design for Broadcom's BCM6010 VDSL transceiver chip consumes less than 2W and operates at -40 to +80°C.

The BCM6010 VDSL transceiver chip provides quadrature-amplitude-modulation (QAM) variable-rate modulation and demodulation, ATM-cell formatting, Reed-Solomon forward error correction, a convolutional interleaver, an on-chip ADC, and an on-chip DAC. Both the reference design and the chip are available today. The BCM6010 chip costs \$24.50 (100,000).

—by Stephen Kempainen

Rockwell Semiconductor, Newport Beach, CA. 1-800-854-8099, 1-949-221-6996, www.rss.rockwell.com.

Circle No. 428

Broadcom, Irvine, CA. 1-714-450-8700, fax 1-714-450-8710, www.broadcom.com.

Circle No. 429

Active sink helps big ICs play it cool

The Pocket Coolers family of fan heat sinks from Aavid Thermal Technologies provides 1.58°C/W heat removal for Socket 7 CPUs and high-power BGA devices. The 7- to 15-mm-high heat sinks use ball-bearing fans with a minimum lifetime of 50,000 hours at 258°C. The clip-mounted Model 3680 targets Socket-7 CPUs and other ICs (the i960, for example). Model 3681, designed for large BGAs, uses brass pushpins that offer high immunity to shock and vibration. The 3682 is a low-profile blower with an aluminum base, designed to cool various embedded mPs that cannot use traditional cooling. Prices are \$9.92, \$13.75, and \$9.23 (1000), respectively. You can order the cooling devices with or without a preapplied interface material.—by Bill Travis

Aavid Thermal Technologies, Laconia, NH. 1-603-224-9988, fax 1-603-223-1738, www.aavid.com.

Circle No. 430



Suitable for portable applications, low-profile fan heat sinks from Aavid provide easy installation and efficient heat removal.

SHARC doubles its bite

The four-year-old, 32-bit, fixed/floating-point 2106x SHARC DSP architecture from Analog Devices has served well in many high-performance DSP applications, especially those requiring multiprocessing. But the DSP industry has recently witnessed significant performance leaps, mainly because DSP suppliers have doubled their cores' execution units. For example, Lucent's (www.lucent.com) DSP 16000 includes two multiply-accumulate (MAC) units, and Texas Instruments' (www.ti.com) C6x contains two nearly identical sets of execution units. Similarly, Analog Devices' new single-instruction-multiple-data (SIMD) SHARC builds on the 2106x and adds a second set of computation units, including an ALU, a data register file, a barrel shifter, and a multiplier. Analog Devices' designers also doubled the buses to allow the core to transfer four 32-bit operands per cycle.

The SIMD SHARC contains a programmable-mode bit that allows you to turn on or off the second set of computation units and execute your legacy SHARC code. When you switch on the second set, the core can still execute SHARC code but simultaneously processes two sets of data. This approach may require you to modify your code by changing the loop count or reordering data in memory.

Although the 2106x and SIMD SHARC have the same cache size and structure, the new architecture can address as much as 8 Mbits of on-chip SRAM, double that of the 2106x. Additionally, the company claims that the SIMD SHARC can operate at frequencies as high as 200 MHz, compared with the 2106x with a 40-MHz maximum operating frequency. Furthermore, at 200 MHz, the SIMD SHARC can perform an FFT as much as 10 times faster than the 2106x.

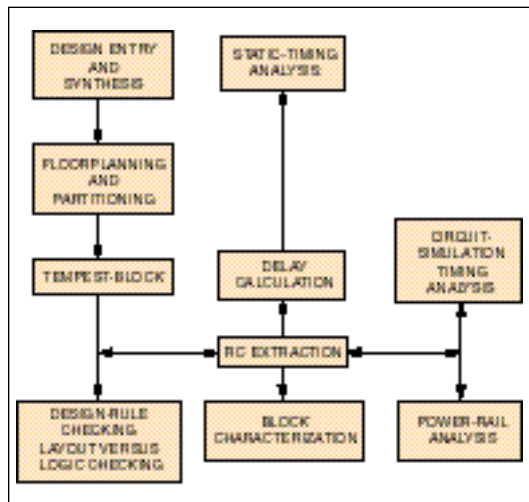
The first device in this new family, the ADSP-21160, targets multiprocessing applications. It operates at 100 MHz with a 2.5V core and 3.3V I/O. In addition to the standard SHARC features, the 21160 contains 4 Mbits of on-chip SRAM; 14 channels of DMA; two time-division-multiplexed serial ports; and a 66-MHz, 64-bit external bus. It supports cluster multiprocessing with six 8-bit-wide, 100-MHz link ports. Analog Devices expects to ship samples in the fourth quarter for \$300.—by Markus Levy

Analog Devices, 1-800-262-5643, www.analog.com.

Circle No. 431

PHYSICAL-DESIGN TOOLS BLOW INTO DESIGNERS' HANDS

The Tempest tool suite from Sycon includes Tempest-Cell for physical-library-cell generation and Tempest-Block for assembling digital-logic blocks. Sycon targets both tools at high-performance, cell-based chip designs. You use Tempest-Cell to generate static-CMOS (no domino-logic circuits) library cells based on a Spice netlist, target-process technology data, and any layout-constraint information. The tool outputs a physical representation of the cell in common intermediate format (CIF), GDSII format, or library-exchange format. Sycon provides cells with as many as 500 transistors and says that Tempest-Cell can in only a few seconds generate a cell containing a few dozen transistors. The tool currently has a text interface, but Sycon expects to offer a graphical user interface by year-end. Although you use Tempest-Cell to rapidly populate a cell library, you still have to validate each cell's performance and generate appropriate models before using the cells in a design.



You use Tempest-Block within your normal physical-block-design flow to create high-density digital blocks with critical cell-placement and interconnect-sensitive constraints.

Tempest-Block also works with a structural Verilog netlist. You use the current version of the tool for control logic and datapath blocks; Sycon is working on a version for memory blocks. Tempest-Block uses Sycon's route-place-route (RoPPro) technology, which first routes all the cells in the core, accounting for expected interconnect-parasitic delays. The tool then places the cells in the core and follows the placement with an additional touch-up routing operation. By using this sequence of layout operations, Tempest-Block lets you design for critical parameters, such as zero-skew clocking or equal-load bus wires. Tempest-Block uses physically based design constraints, such as equal wire lengths for skew control, minimum wire length, and metal widths. Sycon is working on electrically based constraints, including signal-integrity and power design parameters, for a future version of the tool. Tempest-Block output is in CIF and data-exchange format and includes interfaces to Cadence (www.cadence.com) floorplanning and place-and-route tools.

Both Tempest tools run on Unix and Windows platforms. Prices start at \$200,000 for Tempest-Block and \$250,000 for Tempest-Cell.

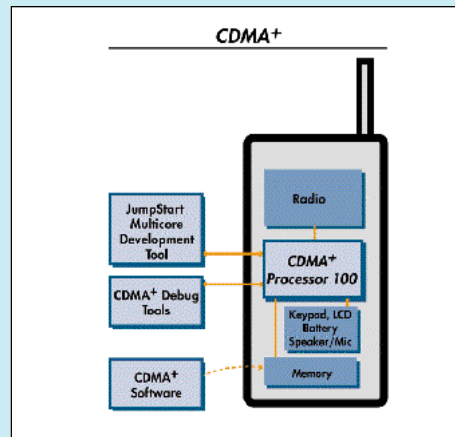
—by Jim Lipman

Sycon Design, Saratoga, CA. 1-408-868-0610, fax 1-408-868-0619, www.sycon-design.com.

Circle No. 432

Competition for CDMA baseband processor emerges

With its CDMA+ Processor 100 chip, VLSI Technology emerges as the only company so far to compete with Qualcomm (www.qualcomm.com) in the market for baseband processors for IS-95 code-division multiple-access (CDMA) mobile phones. The chip integrates an ARM (www.arm.com) processor, an Oak+ (www.dspg.com) DSP core,



VLSI's CDMA+ baseband processor package includes a chip, software, and development tools.

peripherals, an audio codec, a CDMA/advanced mobile-phone-service (AMPS) modem, and voice coders. The chip reuses many of the system blocks that VLSI employs in its third-generation OneC baseband processor.

The CDMA+ software package includes the CDMA and AMPS protocol stack to help designers get their phones working and certified, along with VLSI's JumpStart multicore development tool for integrating ARM and Oak+ software. A CDMA+ development board and debugging tools are also available. Samples are now available, and price will be less than \$20 in volume quantities.

—by Stephen Kempainen

VLSI Technology, San Jose, CA. 1-408-434-3000, www.vlsi.com.

Circle No. 433

Hewlett-Packard has just introduced the latest additions to its Kayak workstation family, which HP based on Intel processors and the Windows NT operating system. The New Kayak XU and XW models are the first in the family to take advantage of the Slot 2 system bus. Slot 2

offers numerous enhancements over Slot 1, which debuted with the original Pentium II ICs. Whereas Slot 1 used cache operating at a much lower speed than the mP to lower cost, the Slot 2 processors feature full-speed cache and high performance. Moreover, Slot 2 supports larger main-memory arrays. Both of the new HP systems can support as much as 2 Gbytes of synchronous DRAM.



A move to the Slot 2 system bus allows the Pentium-II-based HP Kayak XU and XW workstations to leverage full-speed L2 cache, thereby boosting performance.

HP ships the systems with standard dual 10,000-rpm disk drives, a dual-channel SCSI controller, and a RAID (redundant-array-of-inexpensive disks) controller. Both can include one or two Pentium II Xeon processors operating as fast as 400 MHz, and both include the AGP (accelerated graphics port). Electronics designers will likely find the lower cost XU suitable for EDA tasks. Prices for the system start at \$5000, including 3D Labs' (www.3dlabs.com) Permedia 3-D graphics capabilities, which are on the high end of the PC market but more entry level for the workstation market. Prices for the XW start at \$12,000, including HP Visualize, a high-end 3-D-graphics subsystem that HP based on six HP PA-RISC mPs and that can host 50 Mbytes of video memory.

—by Maury Wright

Hewlett-Packard Co., Santa Clara, CA. 1-408-246-4300, www.hp.com.

Circle No. 434

High dynamic range enlightens CMOS image sensor

G-Link's first sensor product, the high-dynamic-range CMOS (HDRC) image-sensor family, delivers high dynamic range, high sensitivity, and high speed that overcome extreme lighting conditions. (The Institute for Microelectronics Stuttgart (www.uni-stuttgart.de/ims/) developed the HDRC image-sensor technology.) Extreme lighting conditions cause image sensors to saturate in bright-light conditions and lose clarity in low-light conditions. HDRC employs a constant contrast resolution in increments of 1% over four decades of intensity to resolve images in poor lighting, making the product useful in security, traffic control, and factory automation.

The 5123256-pixel HDRC 4 image sensor has a constant pixel rate that simplifies data synchronization and all DSP and compression functions. The device supports 120-dB dynamic range, 120 frames/sec, and random access to a pixel or region of pixels. The device uses a 48-pin ceramic SDIP and a single 3.3V supply. Samples are now available for \$40 to \$50 in volume quantities.—by Stephen Kempainen

G-Link, Santa Clara, CA. 1-408-492-9068, www.glinktech.com.

Circle No. 435

Calendar

Aug 16 to 18

Hot Chips 10, Palo Alto, CA, is a symposium that focuses on high-performance chips, systems, and related topics. Topics include RISC, CISC, and VLIW processors; 3-D graphics and multimedia chips; embedded CPUs, chip sets, and DSP chips; special-function chips; low-power chips and technologies; intelligent and high-performance memory chips; field-programmable and reconfigurable chips; compilers and binary translators; benchmarking and performance evaluations; and new technologies. Hot Chips, Los Gatos, CA. Fax 1-408-867-5831, www.hotchips.org.

Vendor voluntarily recalls 60,000 DSOs

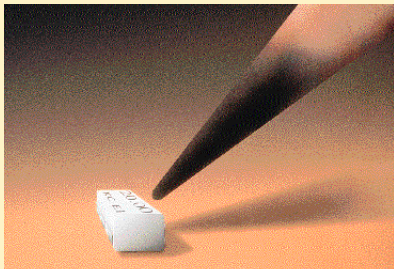
Nobody's been hurt, but somebody could be, and Tektronix (Beaverton, OR) wants to ensure that that doesn't happen. The company is therefore voluntarily recalling approximately 60,000 TDS 210 and TDS 220 digital oscilloscopes. Although they may appear to behave completely normally, scopes that have been damaged through misuse can present a safety hazard. A trace on a pc board inside the scope normally establishes a ground connection, but the connection can open if you accidentally apply a high voltage to a probe's ground lead. You can receive a dangerous shock

if you touch certain points on a scope with a failed ground connection.

The TDS 210 and 220 are 5⁵/₃ 1234¹/₄-in. (approximately), ac-powered benchtop units with black-on-white LCDs. Tek has recalled TDS 210 units with serial numbers below BO49400 or CO10880 and TDS 220 units with serial numbers below BO41060 or CO11175. To receive instructions for returning recalled units, call Tektronix at 1-800-835-9433, ext 2400 or visit the company's Web site at www.tek.com/measurement.—by Dan Strassberg

Flea-sized resonators provide timing in portable apps

Claimed the industry's smallest ceramic chip resonator, the SSR family of surface-mount devices from AVX measures 3.232.131.5 mm. The resonators incorporate load capacitors and are available with an operating frequency of 16



Designed to squeeze into tight quarters in portable equipment, AVX's SSR ceramic resonators offer accurate timing and high shock and vibration resistance.

to 60 MHz ($\pm 0.5\%$ accuracy). Several standard frequencies are available. Maximum resonant impedance is 100V with temperature stability of $\pm 0.3\%$ over operating temperatures of -20 to $+808$ C. Typical price is \$0.30 (100,000).

—by Bill Travis

AVX Corp, Myrtle Beach, SC. 1-803-946-0414, fax 1-803-448-1943, www.avxcorp.com.

Circle No. 437

Programmable-logic design tool: more beef, same price

Remaining at a \$99 bargain-basement price, Cypress' Warp2 programmable-logic-design tool adds three capabilities: You can now input Verilog descriptions, complementing the tool's VHDL capability. A Warp tool supports either HDL. And, with technology Cypress obtained from Aldec (www.aldec.com), Warp2 now provides finite-state-machine (FSM) editing and a timing simulator.

Cypress has developed a synthesis tool for Warp2 that uses automatic module generation that finds recognizable circuits, such as arithmetic and datapath operators, in your code and replaces them with functionally equivalent circuits optimized for the target device. Along with either VHDL or Verilog synthesis, Warp also has a context-sensitive, color-coded HDL editor to help you input your HDL-based design.

The FSM editor lets you graphically describe state machines and generate HDL code from the descriptions. You use the timing simulator on a structural VHDL netlist for delay information. Warp runs on Unix and Windows platforms; you can use the tool with all Cypress programmable-logic devices.

—by Jim Lipman

Cypress Semiconductor, San Jose, CA. 1-408-94-2600, www.cypress.com.

Circle No. 436

PFC dc/dc converters shrink in size, grow in performance

Vicor's second-generation family of high-power-density dc/dc converters have power densities of 80 to 120W/in.³. The 375V-input converters are compatible with power-factor-correcting (PFC) front-end modules. Packages measure 4.632.230.5 in. (1173563 12.7 mm); the packaging provides a stepped profile that allows you to recess the modules into a board cutout for a total aboveboard height of 0.43 in. Cutout mounting also exposes the underside of the converter to airflow for effective heat removal. The modules can accommodate base-plate operating temperatures as high as 1008 C. The 400W V375A5C400A provides a 5V, 80A output at 84% efficiency. The 600W converters are available with outputs of 48V (V375A48C600A; 90% efficiency), 28V (V375A28C600A; 89% efficiency), or 24V (V375A24C600A, 87.7% efficiency). Single-quantity prices are \$180, \$248, \$243, and \$243, respectively.—by Bill Travis

Vicor Corp, Andover, MA. 1-978-470-2900, fax 1-978-475-6715, www.vicr.com.

Circle No. 438