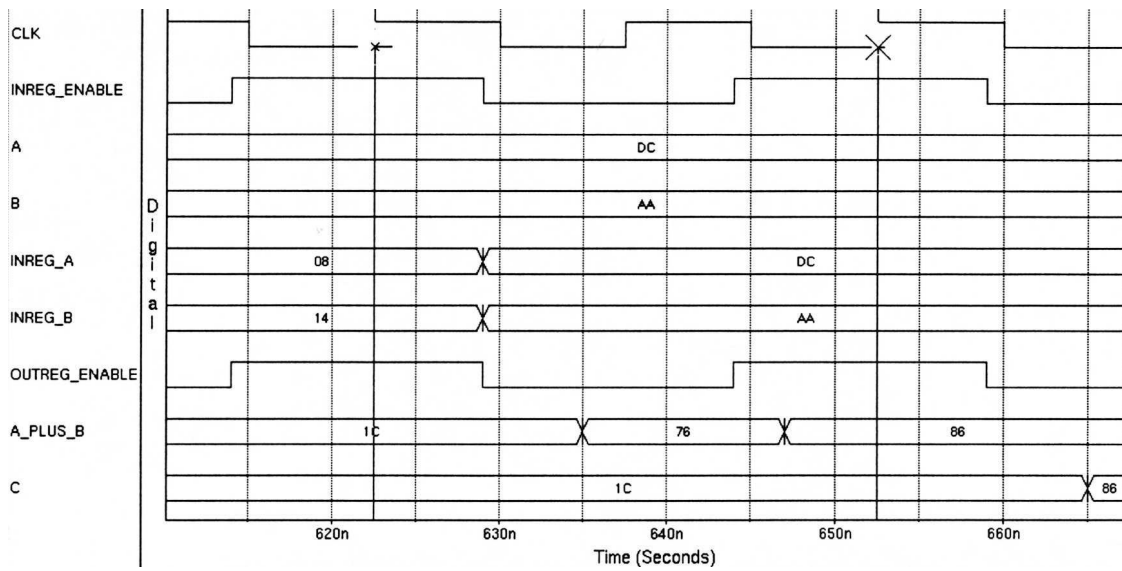


Don't let slow circuits slow down the system Figure 2



This design samples the adder output on the second clock cycle.