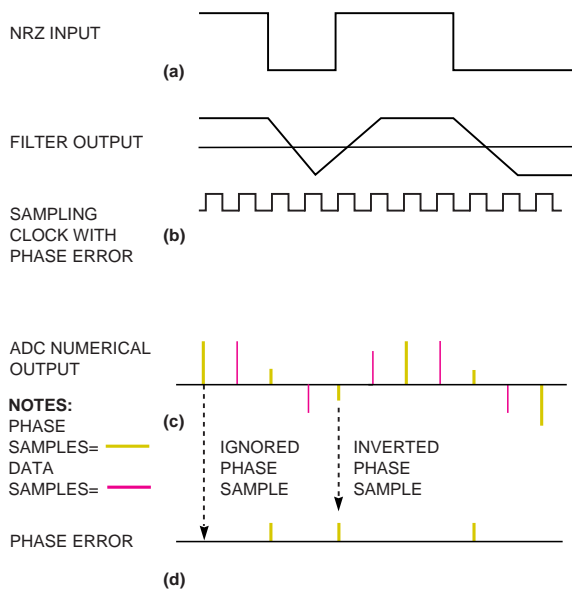


**Figure 3**



**When typical noise-free BCD input data (a) drives an ideal filter, the filter's output (b) consists of a series of positive and negative ramps, each one bit-period long. The ADC samples the filtered output, producing alternating phase and data information at each rising edge of the sampling clock (c). The phase detector ignores phase errors that result from periods without transitions and inverts the necessary phase-error samples (d).**