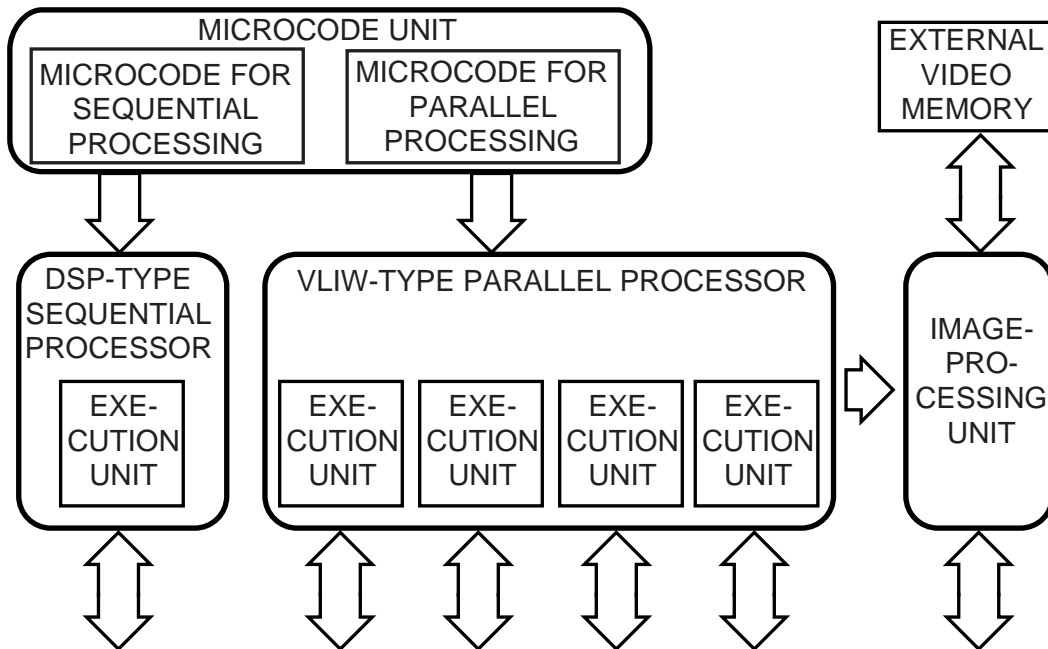


Figure 1



A four-instruction VLIW architecture combines with a DSP to allow the Matsushita MCP to handle tasks such as MPEG-2 video and AC-3 audio decoding, even though the IC operates from a relatively slow, 54-MHz clock.