



SIGNAL INTEGRITY

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Power-plane resonance

Many engineers believe that solid power and ground planes in a digital pc board should act as a large, perfect, lumped-element capacitor. Ideally, a perfect lumped-element capacitor of this size should provide a very low impedance between V_{CC} and ground at very high frequencies (several hundred megahertz and higher). When a gate demands current from the power system, such a capacitor should supply that current with little short-term voltage sag, or droop, according to the rule $dv/dt=I3C$.

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I wish the world were that simple. The problem is, the planes do not form a perfect lumped-element capacitor. Instead, they constitute a distributed system of surprising complexity.

The distinction between a distributed system and a nondistributed (or lumped-element) system involves the relationship between the time delay of the system and the rise time of your signals. As long as the time delay is sufficiently short, you might reason that it hardly affects the results and may be safely ignored. For example, if your pc-board dimensions are 6 in. x 3.6 in., the time delay for signals trapped between the V_{CC} and ground planes, as these travel from one side of the board to the other, is approximately 1 nsec (for an FR-4 substrate). If you are using logic with a rise/fall time in the vicinity of 5 nsec, the lumped-element condition is mostly satisfied, and the planes act, to your benefit, as one large parallel-plate capacitor.

What happens with much faster logic? With 200-psec rise/fall times, the drivers perceive the power-ground structure as a distributed object with a significant delay. This delay causes a number of artifacts. First, during an individual rising or falling edge, only the portion of the planes located within a small radius of the driver can react in time to the power-system noise. The initial noise spike may be much larger than you anticipate. Next, the residual power-system-noise signals from that first event

travel across the board, bump into the edges of the board, reflect, and then finally return, a couple of nanoseconds later, to the driver location. If the driver switches a second time at that precise moment, you see both the old reflected response from the first signal and a response to the second signal superimposed. If the phases add, you get more noise at the second edge than at the first. If the driver continues to act in a repetitive manner (like a clock), the reflected noise builds to a significant degree. This behavior is called a "resonant mode" in the power system. In severe cases, resonance in the power system can cause your product to fail to function.

If your next system design depends on the natural power-plane capacitance to limit power-supply noise, check to see how the round-trip delay across your board compares with your clock period. If it's close, consider using a test board mock-up (just use a plain, double-sided FR-4 core). With this setup, you can directly measure the impedance between the planes using a network analyzer to check for resonances. Another possibility is to take advantage of the latest power-system simulation tools. Several CAD vendors have developed packages that can simulate the distributed nature of a power-plane pair. These packages can help you evaluate the effectiveness of bypass-capacitor placement and can also find resonances due to the shape and configuration of the planes. If you haven't seen this category of tools, ask your CAD vendor for a demo. It's time well-spent (and the 3-D graphics look really cool). e

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