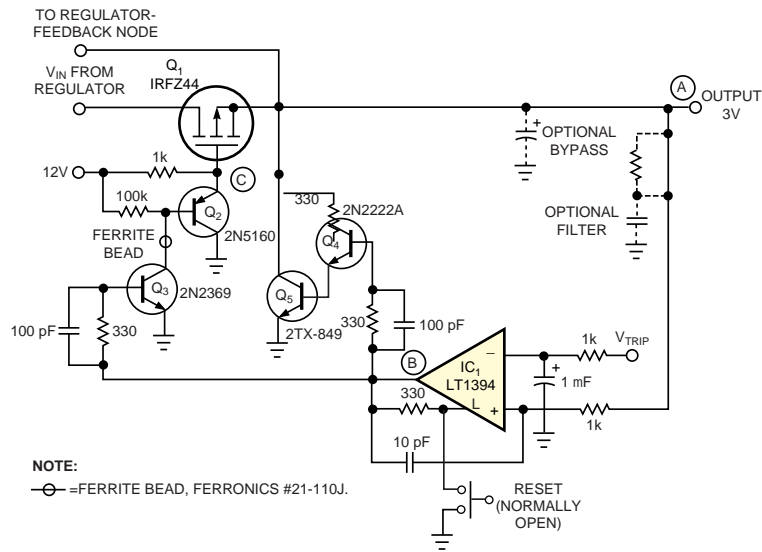
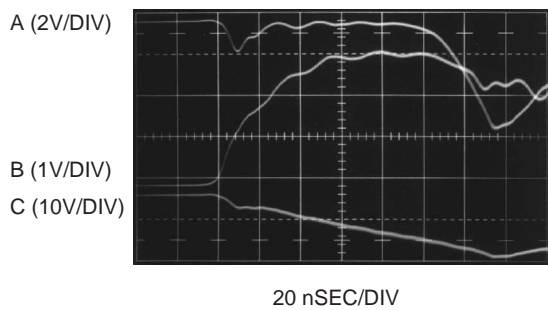


Figure 12



a)



b)

A 20-nsec response-time overvoltage-protection circuit causes IC₁ to latch high, preventing any further output until you reset the circuit (a). The circuit stops the output from going positive in 20 nsec and completely shuts down in 150 nsec (b).