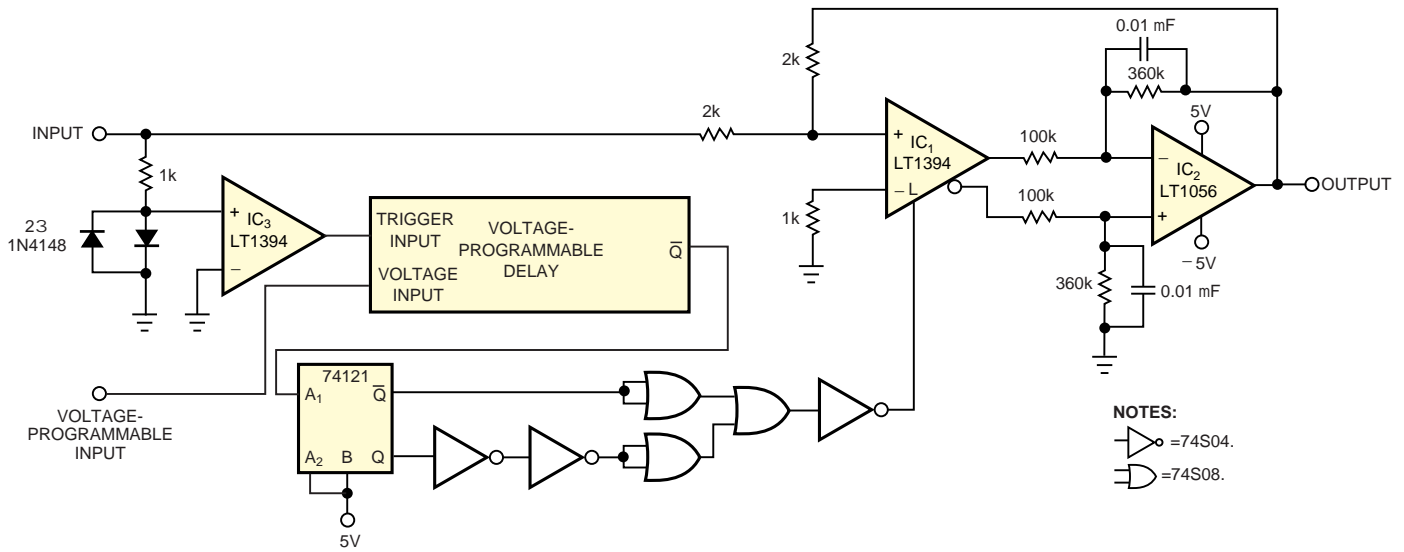


Figure 9



A feedback loop around the comparator and the voltage-programmable-delay circuit allows for controllable sampling of the input and produces a 10-nsec S/H circuit.