

EDN LEADING EDGE

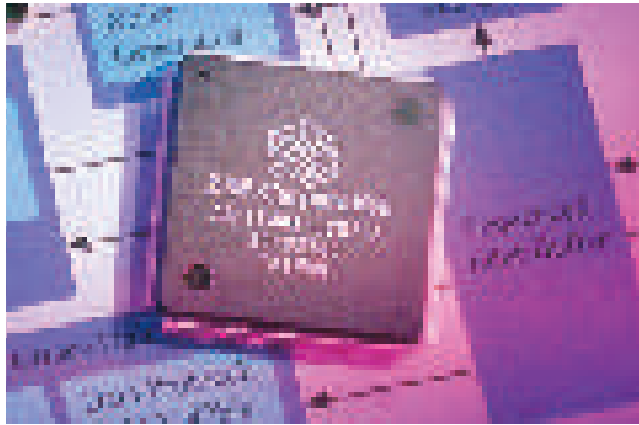
WHAT'S HOT IN THE DESIGN COMMUNITY

EDITED BY FRAN GRANVILLE

Zippy DSP zooms into multichannel-processing zone

ZSP bases a new device, the 16402, on its 16-bit, fixed-point 10X, a super-scalar, RISC-like/DSP architecture that issues as many as four instructions per cycle. It features dual multiply-accumulate (MAC) units and dual ALUs (see *EDN's* "DSP-architecture directory," April 23, 1998, pg 40). The 16402 processes more information channels for voice, video, and data than ZSP's first device, the 16401. The company claims that the processor can simultaneously handle 12 channels of G.723.1, discrete-tone multiple frequency, and echo cancellation.

The 16402 adds support for eight DMA channels, four of which provide automatic interleaving and deinterleaving of H.100/H.110 and most other standard time-division-multiplexed (TDM) buses. The DMA frees the processor from managing complex bus streams. The other four



ZSP's 16402 issues as many as four instructions per cycle and features dual multiply-accumulate units and dual ALUs.

DMA channels can interface to the host-processor interface and the external memory and transfer program and data without stealing cycles from the core. In addition, the 16402's DMA can access the entire internal memory; the DMA on the 16401 can access only the lower 8 kbytes.

The processor has two TDM serial

ports and supports interfacing to almost all standard TDM data streams, including H.100/H.110, ST-BUS, SC-BUS, and MVIP. ZSP adds support for synchronous-burst SRAM and asynchronous memories with a 32-bit bus, whereas the 16401 had only a 16-bit bus. The 16402 also supports as much as 1M word each of external program and data memory.

You can dynamically allocate the chip's 62k words of dual-port SRAM for program and data. The device also provides 2k words of on-chip boot ROM. At 2.5V, the 16402 runs at 200 MHz. It comes in both 17317-mm LPGA and 23323-mm PBGA packages and costs \$65 (10,000).

Currently, only homegrown tools provide support for the ZSP products. For software-tool support, ZSP offers the SDK16i with a Gnu-based optimizing C compiler, an assembler/linker, a debugger, and a simulator/profiler. The optimizing compiler features fixed-point and accumulator data types, intrinsic functions to emulate DSP MAC operations, inline assembly, and pipeline-scheduling information. The simulator profiles code and produces a report on cycle and instruction counts, pipeline efficiency, and instruction usage. ZSP's hardware-developer kit, the HDK16i, handles real-time in-circuit emulation via JTAG and provides visibility into the complete machine state.—by Markus Levy

ZSP Corp, Santa Clara, CA. 1-408-986-1686, www.zsp.com.

Circle No. 397

IC slashes workgroup-hub costs

NeoParadigm Labs has developed a three-port Fast Ethernet switching IC that dramatically lowers cost and maximizes network bandwidth in dual-speed 10/100-Mbps hubs. Targeting workgroup, small-office, and even home-networking markets, the NP313 features three ports that can operate at 10 or 100 Mbps. The IC can switch packets between ports even when two ports are operating at different speeds. The dual-speed support allows an NP313-based hub to connect 10- and 100-Mbps Ethernet segments, leaving the third port available as a cascaded connection to other hubs. Prices range from \$15 to \$25, and the company offers a \$395 evaluation kit.—by Maury Wright

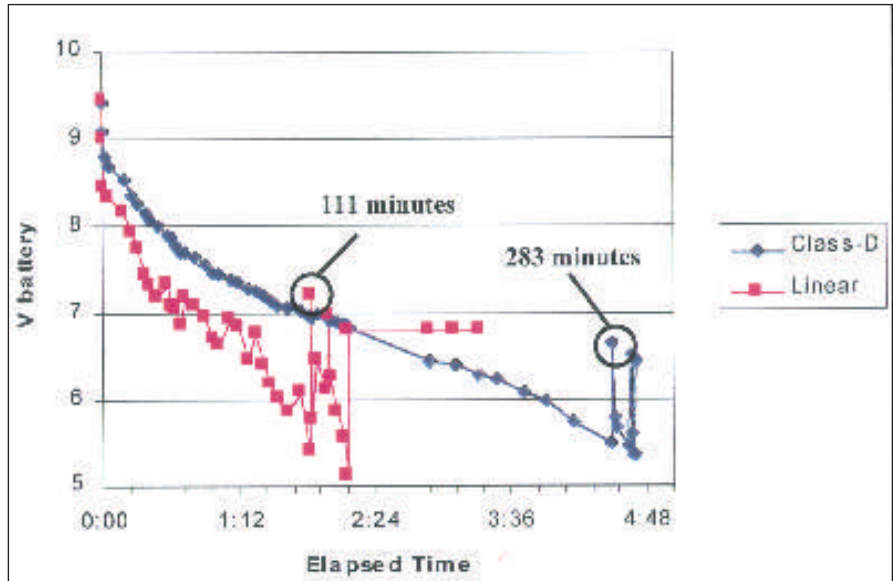
NeoParadigm Labs, San Jose, CA. 1-408-432-0900, www.neoparadigm.com.

Circle No. 398

Class D audio-amp IC scores A+ in efficiency

Texas Instruments has entered the Class D audio-amp arena with its TPA005D02 stereo IC, which can drive speakers with 2W continuous and 5W peak loads. Class D amplifiers offer potentially longer battery life and lower dissipation load than Class A or AB amps (see "Audio-amp ICs get D in class yet still excel," *EDN*, Aug 3, 1998, pg 20). These amps are also attractive as long as they are easy to use and you don't have to compromise performance or component count. With a 5V supply, the 48-pin TSSOP TPA005D02 drives 4V speakers in bridge-tied-load (BTL) configurations with THD plus noise of 0.5% over the audio range; you can also put the IC into a 400-mA shutdown mode. The amplifier inputs accept balanced differential signals and require only a few passive components for output filtering because the IC has both control circuitry and requisite output-power stages.

Efficiency measurement is a gray area with many subtleties. Whereas a Class D unit can achieve efficiencies of 80 to 90% or better for a sine-wave input compared with 25 to 30% for Class AB operation, it's



A side-by-side test using non-sine-wave input signals between the 2W linear TPA0202 and the 2W Class D TPA005D02, shows the approximately 250% increase in effective battery life that this switching audio power amp offers.

more realistic to look at efficiency with non-sine-wave music waveforms. TI set up the TPA005D02 versus its own 2W TPA0202 linear amplifier on a plug&play platform, operating with a 9V alkaline battery and a dc/dc-converter module for the supply rail. Using the "time to first undervoltage lockout" of the dc/dc module as an end-of-test marker, the linear amplifier ran for 111 minutes, whereas the Class D unit ran for 283 minutes, effectively

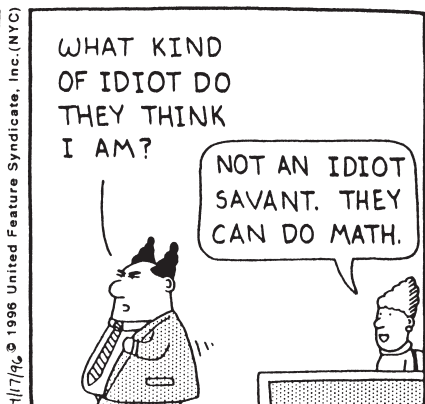
providing a 2.5-times longer battery life.

To help you use the \$3.48 (1000) Class D amplifier, TI also offers the plug&play-compatible SLOP223 evaluation module, which includes a reference design, schematics, and Gerber files.—by Bill Schweber

Texas Instruments Inc, Dallas, TX. 1-800-477-8924, www.ti.com/sc/class_d.htm.

Circle No. 399

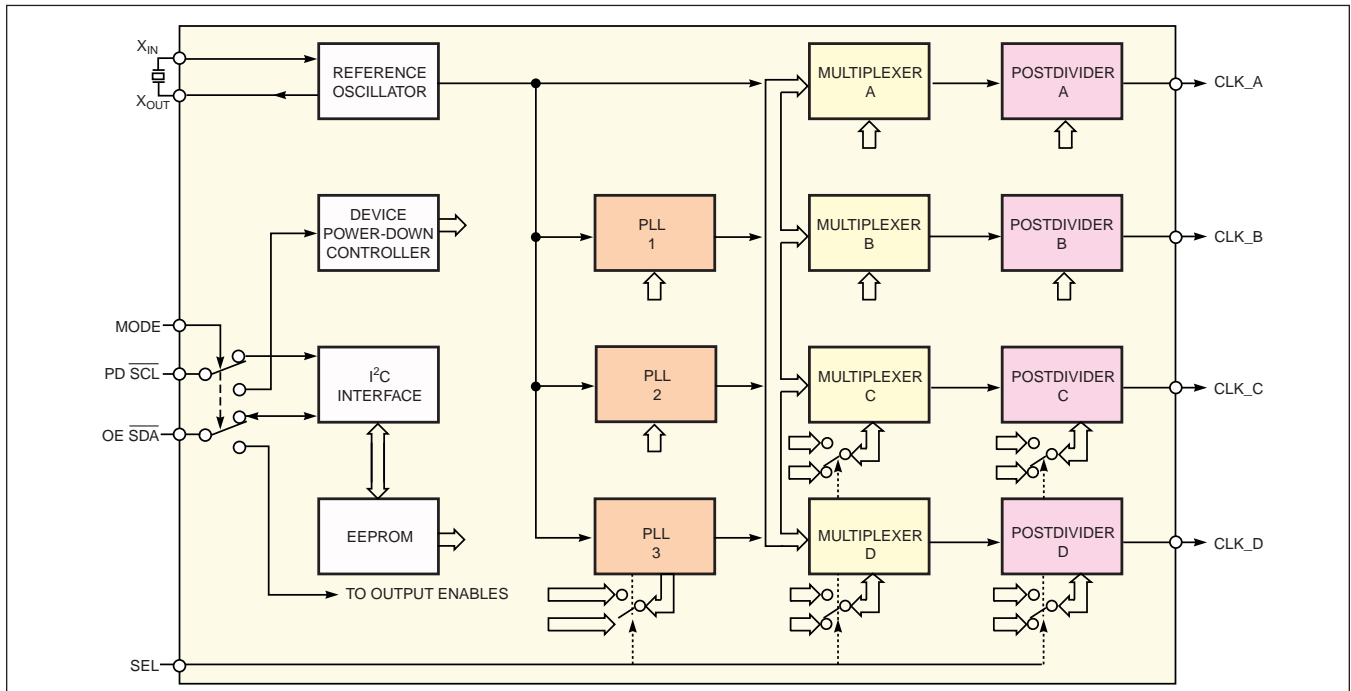
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Program your clock-timing generator in the field



Give field programmability to your timing-generation function by using the FS6370 multifrequency clock-generator IC with its internal EEPROM to set and change division ratios.

American Microsystems' FS6370 multifrequency clock-generator IC lets you program and reprogram its internal division ratios via an internal, 128-bit, serial EEPROM and I²C bus interface. This approach provides an advantage over typical clock-timing generators, which have factory-fixed output frequencies, reducing the flexibility you may need in the final stages of system design of PCs, set-top boxes, and myriad other applications.

The 16-pin IC, for 3.3 and 5V operation, accepts 5- to 27-MHz crystal resonators. It has three independently programmable PLLs, followed by four independently programmable multiplexers and postdividers, so you can develop four precise timing-clock outputs. Should timing requirements change during your design/debugging cycle or the early stages of production, you can change the output frequencies without returning to the factory for a group of preset clock-division ratios. Once your design reaches higher volumes and stability, you

can switch from the EEPROM-based, \$1.75 (25,000) FS6370 to a less expensive ROM-based version.

—by Bill Schweber

American Microsystems Inc,
Pocatello, ID. 1-208-233-4690,
www.amis.com. **Circle No. 400**

Filter ICs provide choice in configuration, order

Two families of switched-capacitor-filter ICs from Maxim give you options in both filter type and order, so you can match their characteristics to your application and use minimal space and external components. The MAX7409 series of fifth-order Butterworth and Bessel filters operate with tunable corner frequencies of 1 Hz to 15 kHz, and a 3100 clock-to-corner frequency ratio. The Bessel variation provides lower overshoot and faster settling time, whereas the Butterworth version offers maximally flat passband response. You can self-clock these 5V, 1.2-mA filters with an external capacitor or use an external clock for greater precision and control. The devices cost 99 cents (1000)

and come in eight-pin DIP and mMAX packages.

For sharper response and cut-off, the MAX7400 series implements eighth-order elliptic response in eight-pin DIP and SO packages. With corner frequencies of 1 Hz to 10 kHz, you can obtain roll-off transition and stopband rejection ratios in 1.5/80-dB or 1.2/58-dB combinations, depending on the model. The 5 and 3V ICs draw 2 mA. You can simply self-clock them or apply an external clock for tighter control, as with their Bessel/Butterworth counterparts. Prices start at \$1.98 (1000).—by Bill Schweber

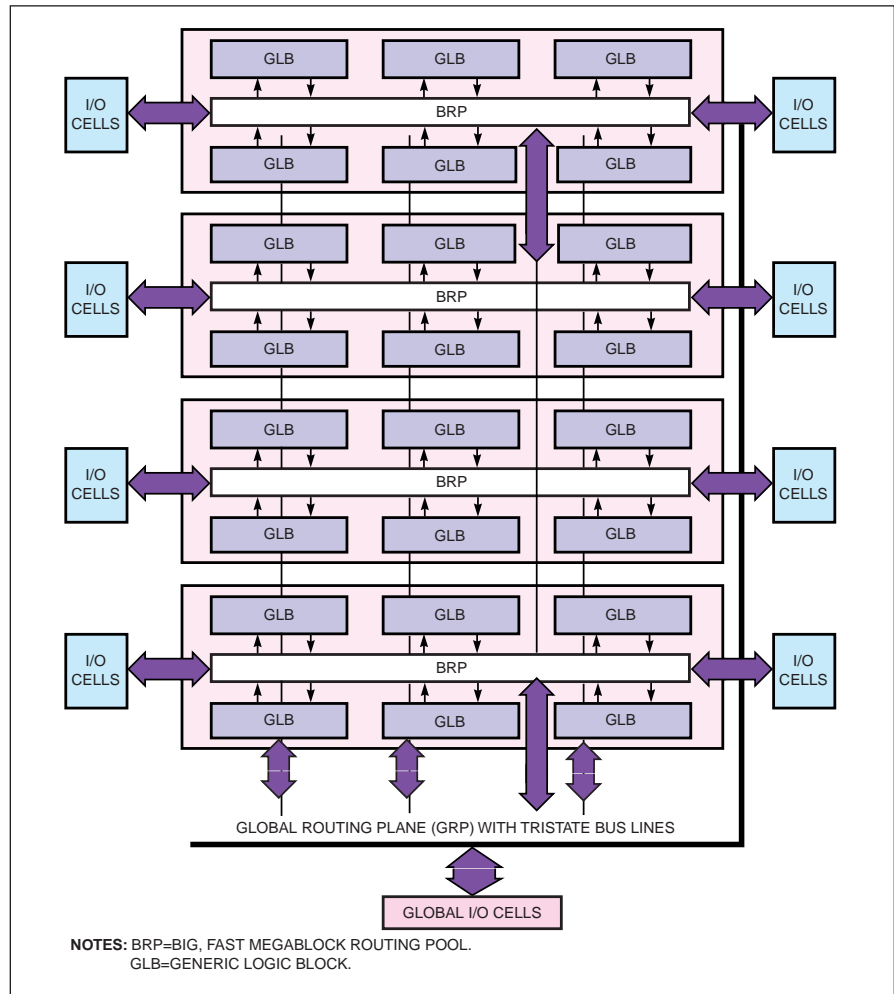
Maxim Integrated Products,
Sunnyvale, CA. 1-737-7600, www.
maxim-ic.com. **Circle No. 401**

Segmented CPLD delivers high logic capacity

With its ispLSI 8000 architecture, Lattice Semiconductor puts a unique twist in that now-familiar path to higher macrocell count. Lattice, like many of its competitors, subdivides the macrocells into multiple sub-arrays the company calls "big, fast megablocks." However, the internal megablock-to-megablock interconnect bus offers true three-state capability instead of emulating this function with logic-consuming multiplexers. Three-state functions are useful when you use the programmable-logic device as a mP peripheral.

Megablocks further subdivide into multiple generic logic blocks, each containing 20 macrocells. Each logic block supports 20 feedback and 24 input terms, and the product-term-sharing array routes as many as 28 product terms to each macrocell. Other macrocell refinements include multiple global clocks and a shared product-term clock option, global and product-term-derived clock enables, separate reset and preset inputs, configurable speed and power, and as many as two outputs—one registered and one combinatorial.

The first member of the ispLSI 8000 family, the ispLSI 8840, costs \$95 (1000) for the -15 speed grade. It offers 840 macrocells and 312 registered, general-purpose I/O signals, each with an optional additional register, in the 432-pin BGA package. The ispLSI 8840 runs at a 5V core



The ispLSI 8000 product family uses hierarchical interconnect to implement its high macrocell counts.

voltage with a 3.3V I/O option and specifies input-to-output propagation times, excluding product-term-sharing, output-rerouting, megablock-to-megablock, and other delays, as fast as 8.5 nsec. The 480-macrocell 8480 and 600-macrocell 8600 will be available by the first

quarter of next year, and the company's road map also includes 3.3V core versions and macrocell counts as high as 1080.—by Brian Dipert
Lattice Semiconductor, Hillsboro, OR. 1-503-681-0118, fax 1-503-681-3037, www.latticesemi.com.

Circle No. 402

REACH US VIA E-MAIL

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Quad USB power-distribution switch controls high side

With the Micrel MIC2527, you can independently control power flow to as many as four Universal Serial Bus (USB) devices. Intended for self-powered USB hub applications, such as monitors, the high-side switches in the 16-pin IC guarantee maximum current of 1.25A per port. Internal

active current-limiting circuitry—featuring greater precision yet lower supply current flow than polyfuses—operate during faulty conditions and eliminate adjacent-channel voltage droop during short-circuit faults. Any overcurrent condition generates a flag signal back to your USB con-

troller. With 200-mV on-resistance, the \$2.22 (1000) MIC2527 is appropriate for 5.1V, 3% supplies; a 100-mV part, the MIC2526, is available for 5V, 3% supply.—by Bill Schweber

Micrel Inc, San Jose, CA. 1-408-944-0800, fax 1-408-944-0970, www.micrel.com. **Circle No. 403**

Prototyping tools and hardware attack SOC designs

The new Velocity Rapid Silicon Prototyping (RSP) system from VLSI Technology combines system-on-chip (SOC) core-integration software with innovative chips and boards. The software and hardware combination gives you a way to develop SOC prototypes using cores from VLSI Technology, third-party vendors, and your own company. Velocity comprises HDL Integrator (HDLi), on-chip buses, RSP chips, and RSP development boards.

The HDLi intellectual-property-delivery tool lets you combine VLSI's cores, libraries, and compilers with cores from other sources. You can mix configurable (soft) and nonconfigurable (hard) cores. The tool also lets you customize high-level reusable blocks, such as IrDA cores and Universal Serial Bus (USB) controllers. HDLi works with Verilog and VHDL and outputs testbenches and synthesis scripts along with your design's HDL description. The tool works with hard cores using a technology-dependent physical layout.

Velocity connects chip cores with three on-chip buses. VLSI enhanced two of ARM's (www.arm.com) AMBA buses,

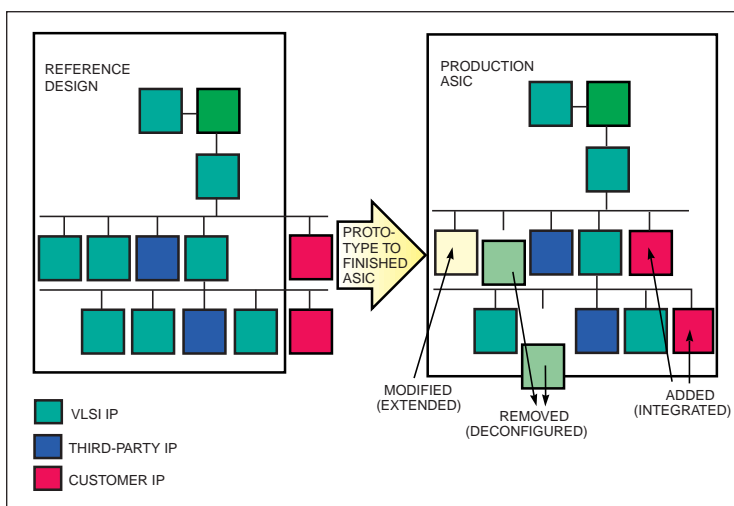
used on ARM's RISC processors. These buses are the AMBA system bus (ASB) for high-speed data transfer and the AMBA peripheral bus (APB) for connecting high-speed cores to peripheral-controller cores. The third Velocity bus is the VLSI On-Chip PCI bus, for PCI connections on your chip.

You implement your RSP chip in Velocity using a chip containing many types of peripheral-controller, timing-controller, and other VLSI and third-party cores along with a processor core. During SOC development, you customize the RSP chip by modifying cores, removing unwanted cores, and adding other required blocks. VLSI designed the first RSP chip, the

RSP7, for general-purpose embedded-system applications. The RSP7, implemented in 0.35- μ m technology, combines a 67-MHz ARM7-TDMI core with general-purpose I/O, USB, infrared, I²C bus, and IEEE 16550 UART blocks. For complete SOC development, VLSI mounts the RSP chip on a pc board with other components and links to external equipment for software development and hardware verification. The first board, the VRSP7, uses the RSP7 chip and is available now.

The VRSP7 board has an RSP7 chip; a 256k \times 32-bit SRAM; a 512k \times 16-bit flash; a 32M \times 32-bit extended-data-out DRAM; a 100,000-gate FPGA; JTAG-debugging; RS-232C, USB, IrDA, general-purpose I/O ports; and wire-wrap space for adding components. VRSP7 costs \$19,000. VLSI brought the RSP7 chip's on-chip buses out to VRSP7 board slots to assist chip-core debugging. VLSI is also developing other boards for data-security, wireless, and set-top-box applications but has not yet announced release dates.

—by Jim Lipman
VLSI Technology, San Jose, CA. 1-408-434-3100, www.vlsi.com. **Circle No. 404**



Rapid Silicon Prototype chips have more features and cores than you need. They all connect on-chip with high-speed, peripheral-core, or PCI buses. You modify, delete, or add cores as required for your system-on-chip design.

DSPs deliver on-chip L2 cache and 2000 MIPS

With the introduction of the \$130, 2000-MIPS C6202, which operates as fast as 250 MHz, Texas Instruments is about to rekindle the flame it lit last year when it introduced the 1200-MIPS TMS320C6201 DSP. The company is also announcing the C6211, the first DSP device to include a Level 2 cache. Although both new devices use the same core and many of the same peripherals as the C6201, TI has made many enhancements.

The C6202 triples the on-chip memory of the C6201 to 384 kbytes, including 256 kbytes of program memory and 128 kbytes of data memory. The program memory divides into two blocks; you can independently access each block, allowing the CPU to fetch a program from one block while a DMA transfer is occurring into or out of the other program-memory block. TI doubled the external bandwidth of the C6202 by adding a second bus that replaces the host-port interface and expands the external-memory interface. The second bus provides a glueless interface to asynchronous FIFO buffers, synchronous-burst SRAM, SDRAM, and external shared-memory devices.

The most interesting feature of the \$25 (25,000) TMS320C6211 is the 64-kbyte L2 cache, which program and data share. TI organized

the L2 cache as four 64-bit-wide banks; you can lock each bank for critical code or data. Experiments at TI have determined that the L2 cache delivers about 80% of the performance of a C62x with infinite memory. You can configure the L2 cache to be direct-mapped or user-configurable for scratchpad RAM or for peripheral data storage on chip.

An L1 data cache access to the L2 cache takes two cycles. Because the line size of the L1 data cache is twice the width of the bus between the cache and the L2, a miss to the L2 requires two accesses. Therefore, a miss from the L1 data cache to the L2 cache takes four cycles to complete if the data is available in the L2. A miss from the L1 program cache to the L2 completes in five cycles. The C6211's 4-kbyte L1 program cache is direct mapped; the 4-kbyte L1 data cache is two-way set-associative. The device has a 256-bit-wide interface between the L1 program cache and the CPU. Two 32-bit buses between the L1 data cache and the CPU can simultaneously access any memory address.

The C6211 has the same peripheral set as the C6201, including two T1/E1 serial ports, two 32-bit timers, and a host-port interface, but lacks an enhanced DMA. Whereas the DMA controller on the 6201 has four programmable channels and a

Calendar

Sept 22 to 25—
Personal Communications Showcase (PCS) '98, Orlando, FL, presents more than 700 exhibitors showcasing personal-communications products. The conference offers more than 30 educational sessions. Topics include wireless Internet, wireless local loop, and voice recognition. The conference package costs \$675 for members of the Personal Communications Industry Association (PCIA) and \$875 for nonmembers. PCS '98 Registration, PCIA, Alexandria, VA. 1-703-739-0300.

fifth auxiliary channel, the enhanced DMA has 16 programmable channels, as well as a RAM space to hold multiple configurations for future transfers. The 6211 also has a direct, 100-MHz interface to SDRAM.—by Markus Levy

Texas Instruments Inc, Dallas, TX. 1-800-477-8924, ext 4500, www.ti.com. **Circle No. 405**

EDN accepts nominations for 1998 Innovation Awards

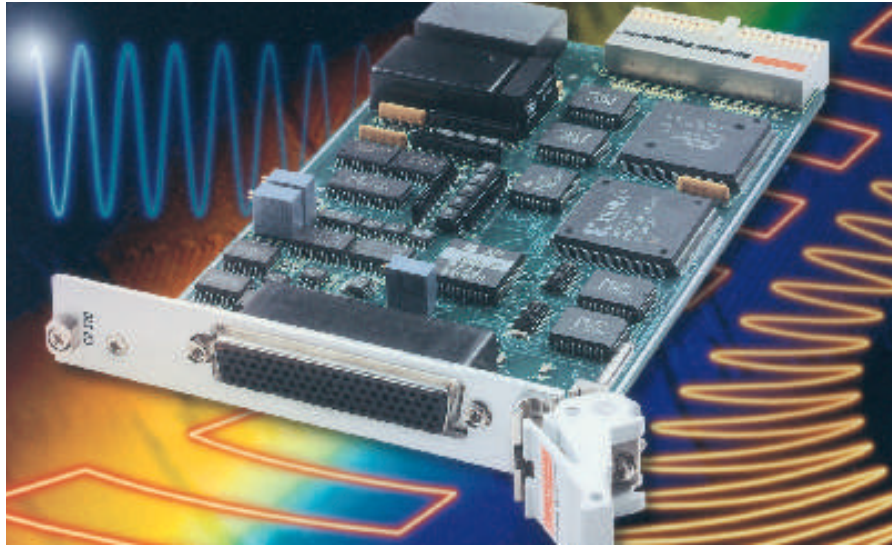
Nominate innovative people on your staff or an exciting product you've introduced over the past year for an *EDN* Innovation or Innovator of the Year Award. *EDN*'s annual Innovation Awards recognize and spotlight excellence and creativity. The Innovator of the Year Award recognizes individuals and groups for innovation in design and technology. The Innovation of the Year Award recognizes unique, state-of-the-art electronics products in nine product categories: digital ICs; analog ICs and discrete semiconductors; micro-processors; test and measurement; EDA tools; computers, boards, buses, and peripherals; components, hardware, and interconnect; embedded development tools; and power sources and controllers. You can nominate any products or technologies introduced and commercially marketed from Jan 1, 1998, through Dec 31, 1998. *EDN*'s technical editors will select the finalists, and you select the winners by voting on our Web site (www.ednmag.com) in February and March. Both the magazine and the Web site will announce winners in May 1999. Deadline for entries is Nov 13, 1998. To order a nomination packet, contact Kathy Leonard at 1-617-558-4405, kathy.leonard@edn.cahners.com, or Lynne M Guimond at 1-617-558-4590, lguimond@cahners.com.

Precision analog controller expands CompactPCI

Responding to the shortage of standard off-the-shelf CompactPCI I/O boards, Pep Modular Computers has developed the CP370 precision analog-I/O signal-conversion controller. Targeting applications in data acquisition and process control, the CP370 is a multifunction data-acquisition module with eight differential or 16 single-ended A/D inputs, four 12-bit analog D/A output channels, and two 16-bit digital I/O ports. Users can configure the A/D converter's unipolar or bipolar inputs and individually program the I/O ports to input or output. The four D/A-converter output channels have separate sense lines.

The analog output channels maintain a relative conversion accuracy of $\pm 0.003\%$ with the help of dedicated board software, a precision reference source, and dedicated D/A converters. A proprietary calibration approach eliminates the need for potentiometers, external reference sources, and postacquisition software-calibration routines.

Pep provides function-setup routines to define I/O operating ranges,



The CP370 CompactPCI data-acquisition module contains eight differential or 16 single-ended analog inputs, four analog outputs and 32 digital I/O bits.

timing sources, and acquisition modes. Test-and-measurement software drivers for HP VEE (www.hp.com) and National Instruments (www.natinst.com) LabView are also available for operation with Windows 95 or NT. The CP370

comes in a CompactPCI 3U form factor, and prices start at \$1314.

—by Warren Webb

Pep Modular Computers, Pittsburgh, PA. 1-412-921-3322, fax 1-421-921-3356, www.pep.de.

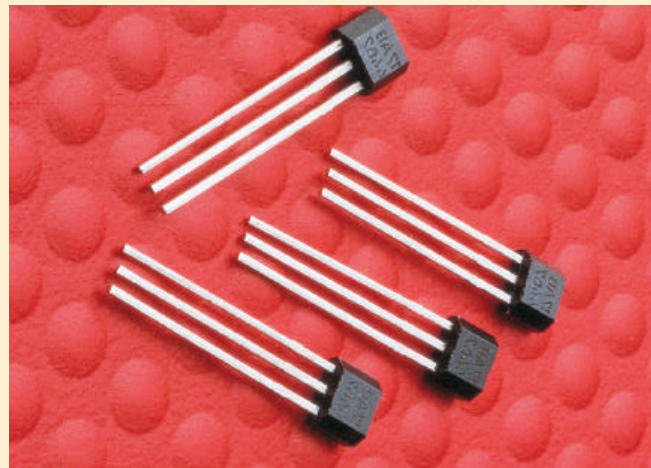
Circle No. 406

IC PUTS TEETH INTO GEAR-POSITION SENSING

The MLX90217, a digital-output, rotary-position gear-tooth sensor, converts movement to a digital signal, thereby allowing a controller to determine speed, distance, or revolutions per minute. The Hall-effect IC from Melexis Inc incorporates an on-chip 10-bit A/D converter and logic that together function as a digital S/H circuit. During signal sampling, the logic recognizes changes in magnetic flux density. The output turns on when the flux reaches its peak and decreases by an amount equal to the built-in hysteresis. Similarly, the output turns off after the flux reaches its minimum value and then increases by an amount equal to the hysteresis. The MLX90217 satisfies all DIN EMC requirements for automotive-battery applications. The IC comes in a three-pin SIP and costs \$1.16 (10,000).

—by Bill Travis

Melexis Inc, Webster, MA. 1-508-943-9430, fax 1-508-943-0487, www.melexis.com. **Circle No. 407**



An A/D converter and logic form a digital S/H circuit in the MLX90217 gear-tooth-position sensor from Melexis.