

Fast comparators find their niche in linear applications

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Comparators may be the most underrated and under-used monolithic linear components—an unfortunate fact because comparators are also among the most flexible and universally applicable components. The comparator's lack of recognition is largely thanks to the IC op amp, whose versatility allows it to dominate analog design. Although you can look at comparators as devices that crudely express an analog signal in digital form, specifically as a 1-bit A/D converter, this viewpoint is wastefully constrictive.

Comparators, and high-speed comparators in particular, can implement linear-circuit functions that are as sophisticated as any op-amp-based circuit. A recently introduced comparator, the LT1394 (see sidebar "High-speed comparator pairs high speed with stability"), combined with the precautionary tales for all high-speed components, permits fast linear-circuit functions that are difficult or impractical to perform using other approaches.

Some of the following applications represent the state of the art for a particular circuit function. Others show simplified or improved ways to implement standard functions by using the comparator's easily accessible speed. All of the circuits have been carefully (and painfully) worked out and should serve as good ideas for high-speed comparators and their uses.

Switchable-output crystal oscillator

In Figure 1, a basic oscillator configuration with additional circuitry permits logic commands to electronically switch between crystals. Oscillation is possible only when one of the logic inputs is high. The 1-kV resistors at the comparator's input set the dc bias point. The 2-kV, 75-pF path sets up phase-shifted feedback, and the circuit resembles a wideband unity-gain follower at dc. The selected crystal path provides reso-

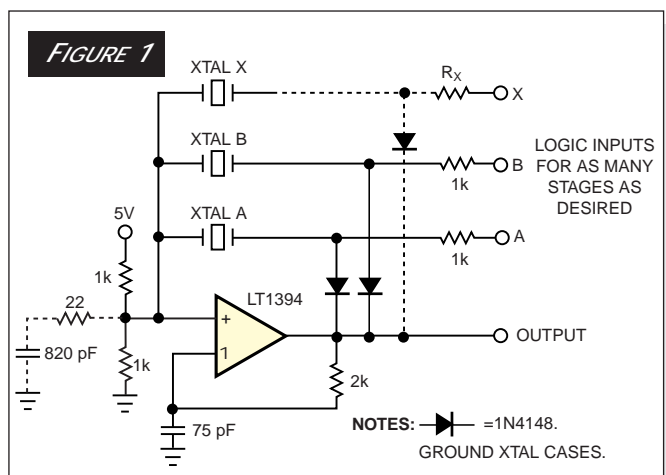
Comparators don't "just compare" in the same way that op amps don't "just amplify." A collection of application circuits demonstrates just how flexible and useful a high-speed comparator can be.

nant positive feedback, and stable oscillation occurs. The basic circuit supports oscillation frequencies from 1 to 10 MHz. At higher than 10 MHz, AT-cut crystals operate in overtone mode, and oscillation can occur at multiples of the desired frequency. If you include the optional

dampener network at the comparator input, the circuit can support oscillation frequencies as high as 30 MHz. This network rolls off gain at high frequencies, ensuring proper operation.

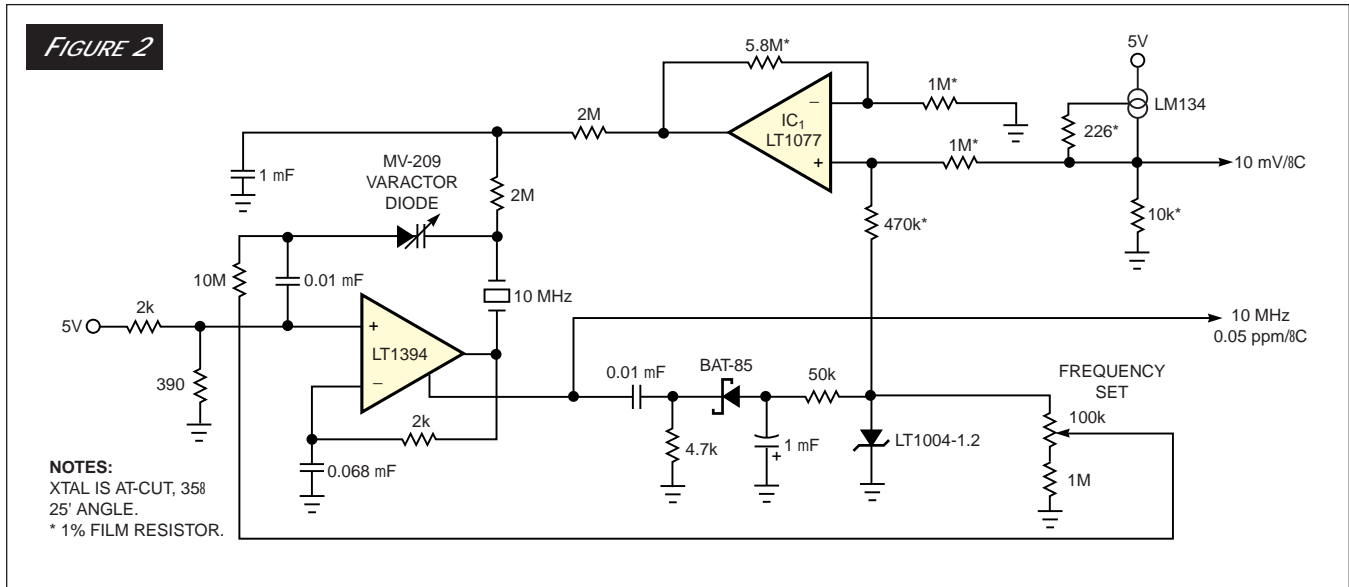
Temperature-compensated crystal oscillator

Figure 2 depicts a temperature-compensated crystal oscillator. This circuit reduces the oscillator's temperature drift by



Biasing one of the logic inputs high places the associated crystal in the feedback path to make a switchable-output crystal oscillator.

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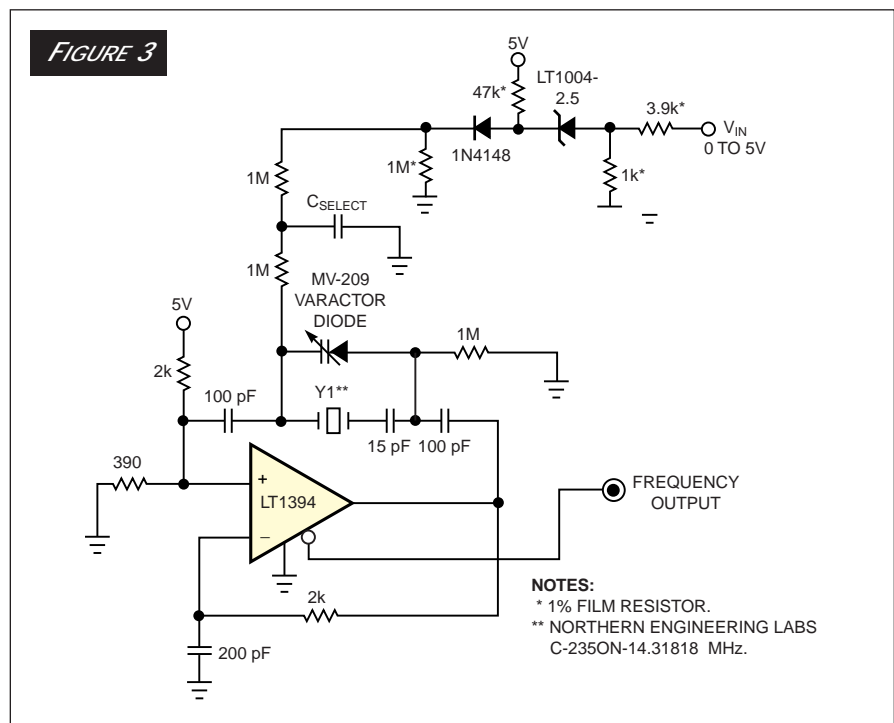


The temperature-dependent bias of the varactor diode reduces this 10-MHz crystal oscillator's drift by 20 to 1.

inserting a temperature-dependent compensatory correction into the crystal's frequency-trimming network. This open-loop correction technique relies on matching the oscillator's frequency-versus-temperature characteristic, which is repeatable.

The LT1394 and associated components form the crystal oscillator, which operates similarly to the circuit in **Figure 1**. The LM134, a temperature-dependent current source, biases IC₁. The dc level at the positive input of IC₁ is a function of the LT1004's reference voltage and the LM134's temperature-dependent voltage. IC₁ amplifies the resultant dc level at its positive input by a gain of approximately 7. The circuit derives the LT1004's negative bias voltage from the oscillator's output, thereby maintaining the circuit's single-supply operation. This arrangement delivers temperature-dependent bias to the varactor diode, causing a scaled variation in the crystal's resonance versus ambient temperature. The varactor's bias-dependent capacitance shifts the crystal's frequency to complement the circuit's temperature drift. This compensation provides a simple, linear, first-order correction.

The circuit corrects for the crystal's -70-ppm frequency shift over 0 to 70°C within a few ppm. The frequency-set trim also biases the varactor, allowing accurate output-frequency setting. Even better compensation is possible by



Another variant of the basic crystal oscillator permits tuning of a 43NTSC subcarrier (14.31818 MHz) by more than ±240 ppm (±4 kHz).

including nonlinear terms in the temperature-to-voltage conversion.

Voltage-controlled crystal oscillator

Another variant of the basic crystal oscillator permits voltage-tuning of the output frequency (**Figure 3**). Such voltage-

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controlled crystal oscillators are useful when a slight variation of a stable carrier is necessary. The most common application is to provide a 43NTSC sub-carrier tunable oscillator suitable for phase locking.

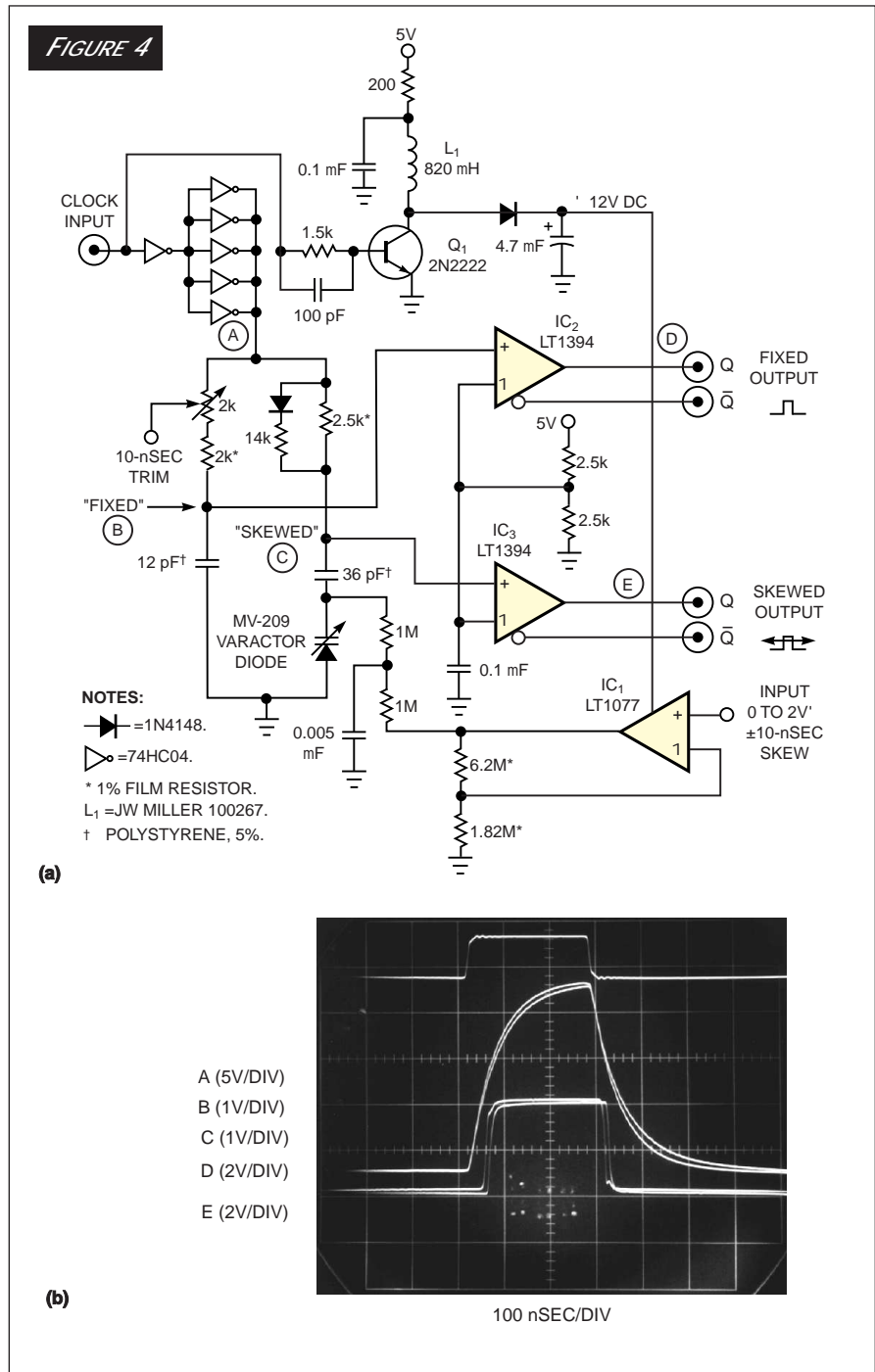
This circuit again configures the comparator and associated components as a crystal oscillator. The tuning input, V_{IN} , biases the varactor diode. The tuning-network arrangement allows a 0 to 5V drive to provide a reasonably symmetric and broad tuning range around the 14.31818-MHz center frequency. The capacitor C_{SELECT} sets the tuning bandwidth. You should select the value of this capacitor to complement the loop response in phase-locking applications. The tuning deviation from the 43NTSC 14.31818-MHz center frequency exceeds approximately ± 240 ppm (± 4 kHz) for a 0 to 5V input.

Tunable clock-skew generator

It is sometimes necessary to generate pairs of identical clock signals that are phase-skewed in time. Further, you may desire to set the amount of time skew via a tuning voltage. Figure 4a's circuit performs both functions by using comparators to digitize phase information from a varactor-tuned time-domain bridge. A 0 to 2V control signal provides approximately ± 10 -nsec of output skew. The input drives the CMOS inverters, which in turn deliver noninverting drive to the bridge network (Trace A, Figure 4b). (The bridge, which essentially comprises two RC sections, responds in ramp fashion at both of its outputs; Trace B is the bridge's "fixed" output, and Trace C is its "skewed" output.) A varactor diode, which receives bias from IC_1 and hence from the control input, tunes the capacitance of the "skewed" half of the bridge.

The comparators, which the circuit references to one-half the supply voltage, trigger when their positive inputs exceed the reference point. Traces D and E are the outputs of IC_2 and IC_3 , respectively. The imbalance in the bridge's RC time constants, which the voltage input controls, determines the time skew of the comparators' responses. The diode-resistor network across the 2.5-kV bridge resistor compensates for ramp-induced variation of varactor capacitance, enhancing control symmetry.

Q_1 and associated components form a simple voltage-



Comparators IC_2 and IC_3 extract phase-difference information from the varactor-tuned bridge to implement a voltage-tunable clock-skew generator (a). Waveforms show the fixed and skewed outputs, traces D and E, respectively (b).

boost stage, enabling IC_1 to supply adequate varactor bias. The bridge's ratiometric operation permits almost 100-to-1 power-supply rejection ratio over a 4.5 to 5.5V input range. To trim this circuit, put in 2V and adjust the 2-kV potentiometer for 10 nsec of skew in the outputs. Over a 0 to 2V

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range, output skew varies continuously from -10 nsec through 0, to 10 nsec.

Fast, high-impedance, variable-threshold trigger

Instrumentation applications frequently require a fast trigger with a variable threshold. A high-impedance input is also often necessary (Figure 5). Comparator IC₁ is the basic trigger; the V_{TRIGGER} input sets the threshold at IC₁'s negative input. Source follower Q₁ provides high impedance with approximately 2 pF of input capacitance and 50 pA of bias current. Normally, Q₁'s source bias point is uncertain and drifts, but stabilization techniques eliminate this concern.

IC₁ measures filtered versions of Q₁'s gate and source volt-

Buffer Q₂ provides a 2-pF, 50-pA high-input-impedance characteristic to IC₁'s fast trigger. V_{TRIGGER} adds a variable threshold at the comparators' negative input.

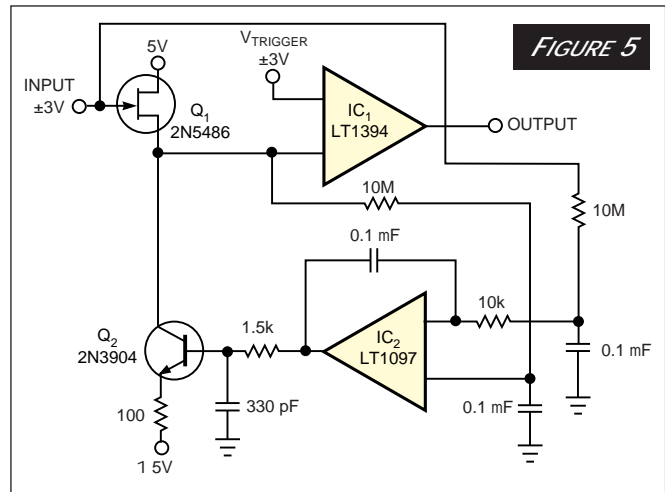
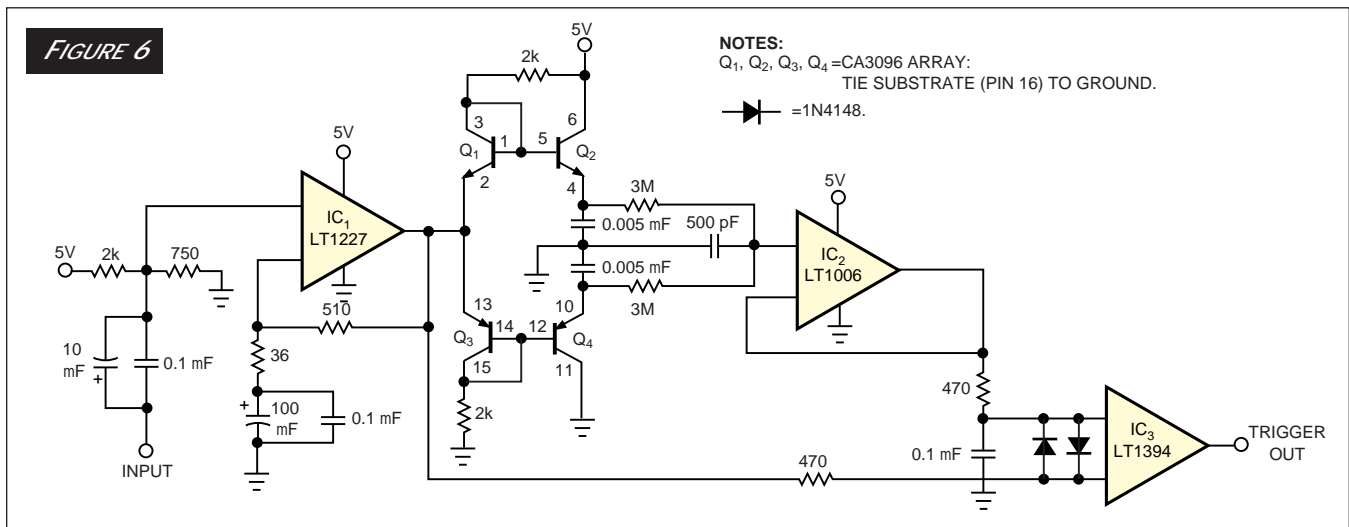


FIGURE 5

**NOTES:**

Q₁, Q₂, Q₃, Q₄=CA3096 ARRAY:

TIE SUBSTRATE (PIN 16) TO GROUND.

—▷ = 1N4148.

In this 45-MHz, single-supply adaptive trigger, the output comparator's threshold varies ratiometrically with the input amplitude to maintain data integrity over a more than 85-to-1 input-amplitude range.

HIGH-SPEED COMPARATOR BASICS

The LT1394 comparator has a 200-GHz gain bandwidth and a 7-nsec response time. It features TTL-compatible complementary outputs, a latch pin, and good dc-input characteristics. The comparators' outputs directly drive all 5V logic families, including the high-speed ASTTL, FAST, and HC parts. TTL outputs make the device easy to use in linear applications for which ECL output levels are often inconvenient.

This comparator is less prone to oscillation and other vagaries than some

slower comparators, even those with slow input signals. The LT1394 is particularly stable in its linear region. Also, output-stage switching does not appreciably change power-supply current, further enhancing stability.

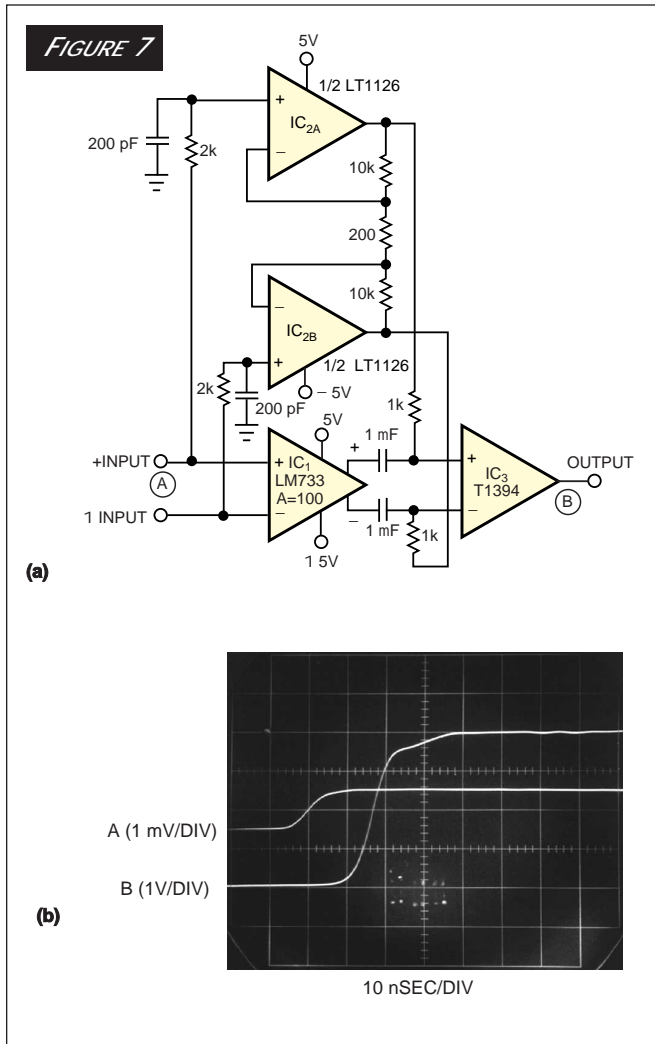
Unfortunately, laws of physics dictate that the circuit *environment* in which the comparator works must have the proper preparation. Parasitic effects, such as stray capacitance, ground impedance, and layout, often limit the performance of high-speed circuitry. To create the

best operating environment and make accurate measurements, you need to know not just how high-speed comparators operate, but also how equipment, cables, connectors, probes, terminations, and layout affect their performance (Reference A).

Reference

A. Williams, Jim, "A seven-nanosecond comparator for single supply operation," Application Note 72, Linear Technology Corp, 1998.

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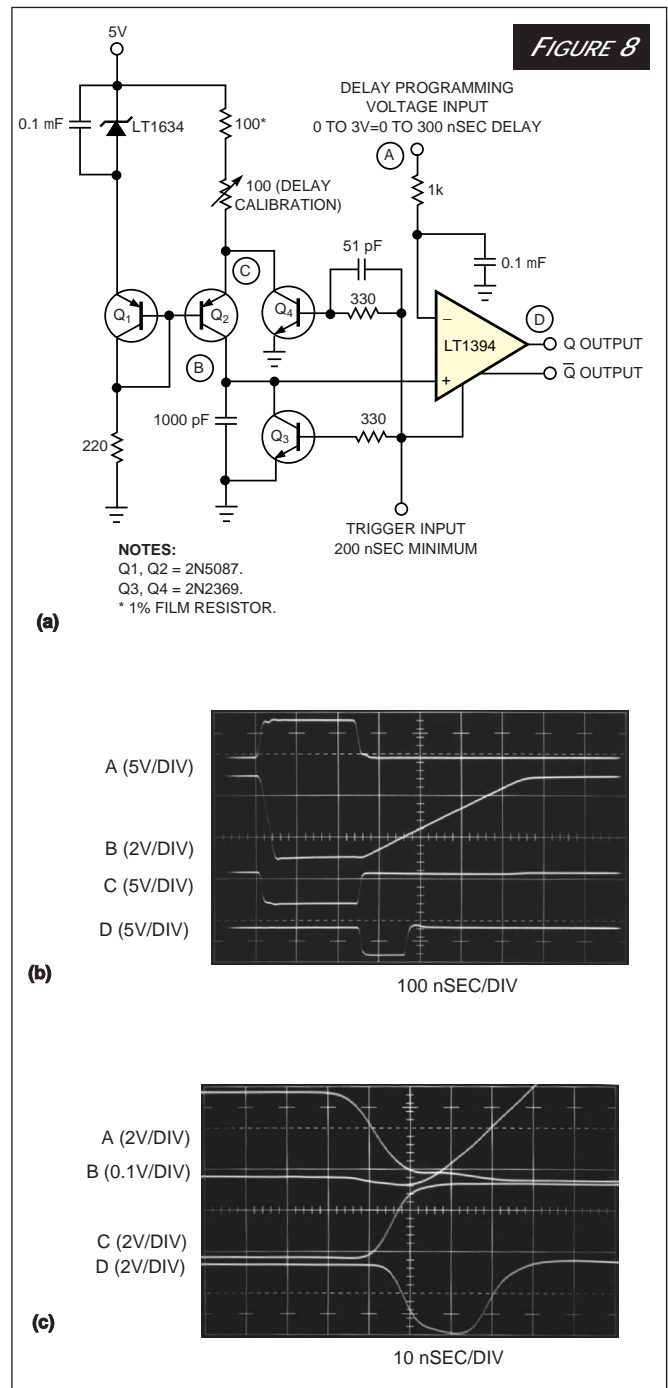
Preamplifier IC₁ with added dc correction from IC_{2A} and IC_{2B} (a) allows comparator IC₃ to respond to a 500-mV overdrive in 18 nsec (b).

ages. IC₂'s output biases Q₂, forcing Q₁'s channel current to whatever value is necessary to equalize IC₂'s inputs and, hence, Q₁'s gate and source voltages. IC₂'s input filtering and roll-off are far slower than input frequencies of interest but do not interfere with the circuit's main signal path. The 330-pF capacitor prevents fast edges that couple through Q₂'s collector-base junction from influencing IC₂'s operation.

Q₁ contributes negligible timing error to minimize overall delay; Q₁'s source lags behind the input by only 300 psec. The delay from the input to IC₁'s output is approximately 8 nsec.

High-speed adaptive-trigger circuit

Line and fiber-optic receivers often require an adaptive trigger to compensate for variations in signal amplitude and dc offsets. The circuit in Figure 6 triggers on 2- to 175-mV signals from 100 Hz to 45 MHz and operates from one 5V rail. IC₁, operating at a gain of 15, provides wideband ac gain. The

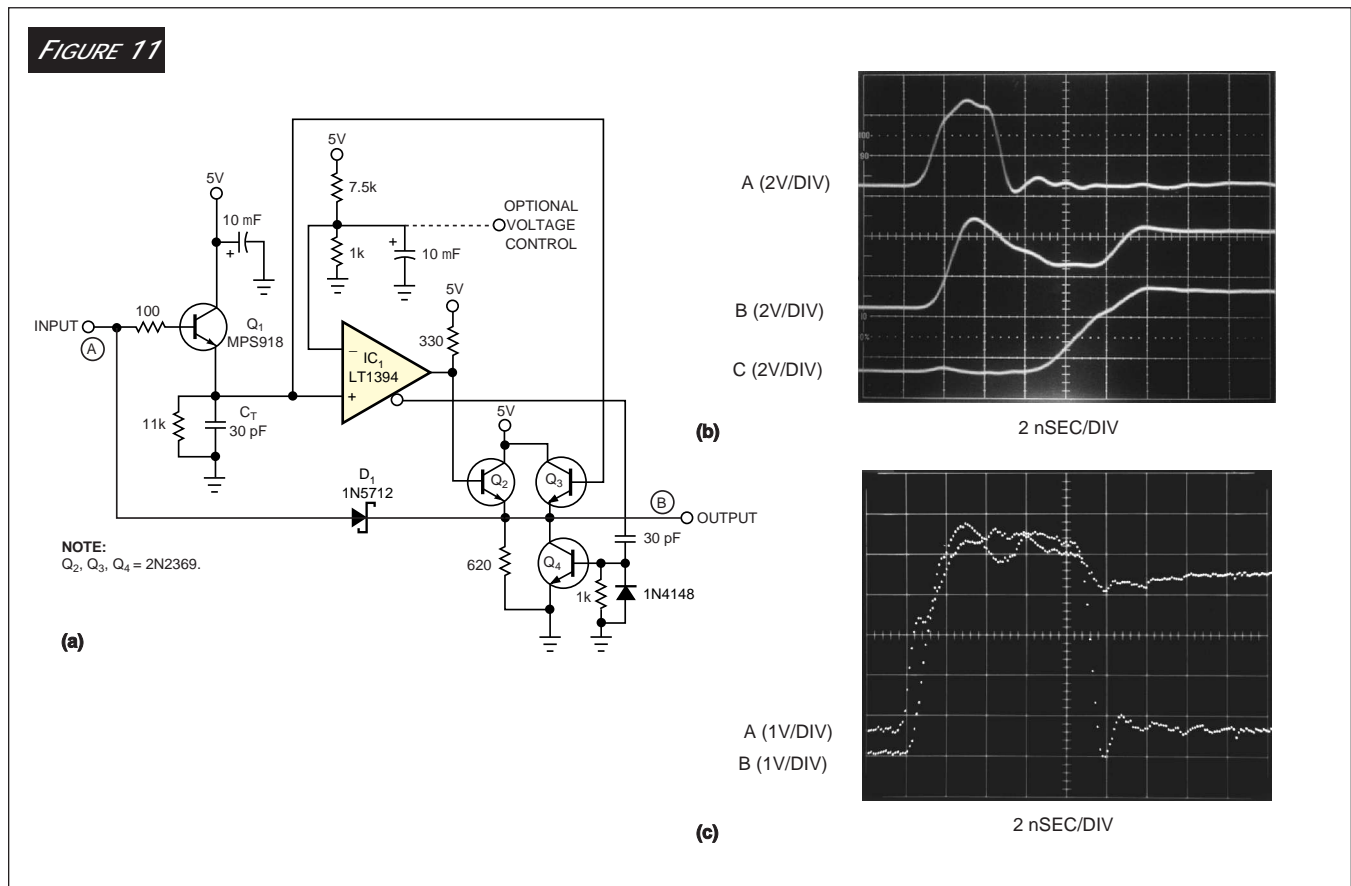


Pairing an emitter-switched current source with a fast comparator (a) produces a fast voltage-controlled-delay circuit with a precise delay time (b). Expanded waveforms (c) show the exact timing relationships.

output of this stage biases a two-way peak detector comprising Q₁ through Q₄. Q₂'s emitter capacitor stores the maximum peak, and Q₄'s emitter capacitor retains the minimum excursion. The dc value of the midpoint of IC₁'s output signal appears at the junction of the 500-pF capacitor and the

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FIGURE 11



A high-speed pulse stretcher has subnanosecond rise and fall times (a). Disconnecting the feed-forward path that originates at C_T (b) shows that the output sags for 8 nsec (Trace B) before C_T can restore its amplitude (Trace C). In a 3.9-GHz bandpass (c), the output amplitude (Trace B) drops when the input (Trace A) decays, but the circuit maintains a high logic level.

C₁ and Q₁ through Q₄ form a delay-programming voltage identical to the one in Figure 8a. Q₅, the LT1082 switching regulator, and associated components constitute the avalanche pulse generator. The generator provides an 800-psec pulse with rise and fall times within 250 psec. Pulse amplitude is 10V with a 50V source impedance.

The pulse generator requires high-voltage bias for operation. The LT1082 switching regulator forms a high-voltage switched-mode control loop. This regulator pulse-width-modulates at its 40-kHz clock rate. The circuit rectifies L₁'s inductive events and stores the result in the 2-mF output capacitor. The adjustable resistor-divider provides feedback to the LT1082. The 10-kV 1-mF RC network provides noise filtering.

The circuit applies the high voltage to Q₅, which is a 40V breakdown device, via the R₁/C₁ combination. You should set the high-voltage bias-adjust control at the point when the free-running pulses across R₂ disappear. This setting puts Q₅ slightly below its avalanche point. Applying IC₁'s output pulse to Q₅'s base causes Q₅ to go into avalanche. The result is a quickly rising, fast pulse across R₂. IC₁ discharges, Q₁'s collector voltage falls, and breakdown ceases. IC₁ then recharges to just below the

avalanche point. At IC₁'s next pulse, this action repeats.

Figure 10b, taken with a 3.9 GHz bandpass instrument (Tektronix 661 with 4S2 sampling plug-in) shows circuit detail. Trace A is IC₁'s output, and Trace B is the avalanche pulse. When avalanche occurs, Q₅'s reverse base current rises so abruptly that IC₁'s output cannot directly absorb it. The 100V resistor and the ferrite beads allow C₁ to handle the transient load. Without this network, IC₁'s positive-going output reverses direction and rings severely before completing its transition, corrupting avalanche behavior. Even with these components, artifacts of the avalanche-induced base current are visible in IC₁'s output trace.

The avalanche pulse measures 8V high with a 1.2 nsec base. Rise time is 250 psec, and fall time is 200 psec. In reality, the times are probably slightly faster, because the oscilloscope's 90-psec rise time influences the measurement.

You may have to select Q₅ for avalanche behavior. Although such behavior is characteristic of the specified device, the manufacturer does not guarantee it. A sample of 50 Motorola 2N2369s, spread over a 12-year date-code span, yielded 82%. All "good" devices switched in less than 600 psec. This circuit also requires the selection of C₁ for a 10V amplitude output; the value spread is typically 2 to 4 pF.

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Ground-plane-type construction with high-speed layout, connection, and termination techniques is essential to obtain good results from this circuit.

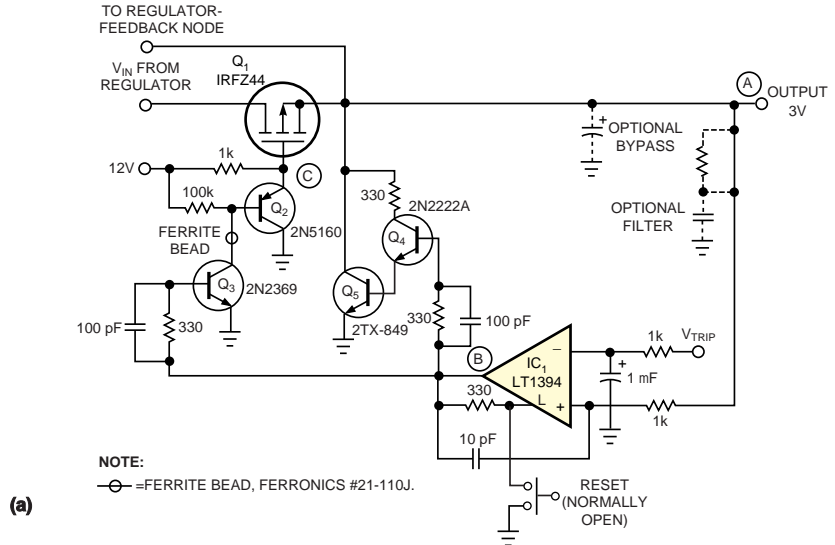
Fast pulse stretcher

A pulse stretcher requires a minimum input-pulse width of 5 to 10 nsec to operate. The rise and delay times are of the same order. **Figure 11a**'s circuit is considerably faster. This circuit produces a stretched pulse from a 2-nsec width input with rise and delay times of 650 psec.

The input pulse causes Q_1 to conduct, which charges the timing capacitor, C_T . The input pulse also feeds forward around IC_1 , via D_1 , to the output. Additionally, Q_3 buffers C_T 's potential, which also feeds forward to the output. IC_1 responds to C_T 's charging by going high, which turns on Q_2 , and augments the output's high state. IC_1 's 7-nsec delay does not affect output delay or waveshape because the feed-forward paths "fill in" the dead time before the comparator responds. The output pulse is a composite of the input and comparator-based responses. The small change in output amplitude when the input ceases is not deleterious. When the input pulse falls, IC_1 's output remains high until C_T discharges below IC_1 's negative input. When IC_1 goes low, its inverting output goes high, pulsing Q_4 to pull the output down in 5 nsec.

The feed-forward paths are crucial to the circuit's operation. The effect of D_1 's path is easy to understand, but the route that originates at C_T is less obvious. A good way to see the effect of C_T 's path is to eliminate it. By opening Q_3 's base, you can reveal this path's effect (**Figure 11b**). Trace A is the input pulse; Trace B, the output; and Trace C, IC_1 's output. The absence of the C_T -based feed-forward path is evident. The output (Trace B) sags for 8 nsec before the comparator responds and restores output amplitude.

Evaluating circuit operation requires a fast pulse generator and a wideband oscilloscope. **Figure 11c** shows the pulse stretcher's input/output relationship in a 3.9-GHz sampled bandpass. As in **Figure 11b**, Trace A is the input pulse, and Trace B is the output. The output amplitude drops slightly when the input ceases, but the logical high state is maintained. Also visible on the input's leading edge is a 0.5V-amplitude, 500-psec aberration, which occurs at about 3V into the transition. This aberration results from the circuit's nonlinear input impedance. The aberration occurs above a

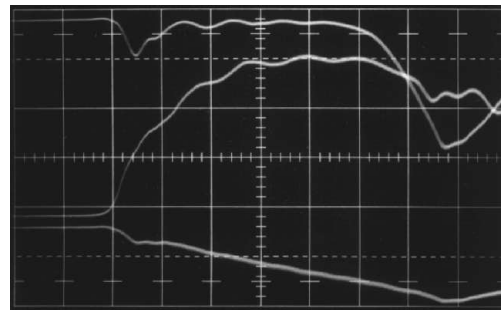
FIGURE 12

(a)

A (2V/DIV)

B (1V/DIV)

C (10V/DIV)



20 nSEC/DIV

(b)

A 20-nsec response-time overvoltage-protection circuit causes IC_1 to latch high, preventing any further output until you reset the circuit (a). The circuit stops the output from going positive in 20 nsec and completely shuts down in 150 nsec (b).

logical high level and is acceptable. The output is delayed from the input by only 650 psec, and rise time is also approximately 650 psec.

The output-pulse width approximately equals the input-pulse width that you add to 25 nsec/pF of C_T 's value. The ratiometric biasing of IC_1 's inputs provides supply-variation immunity of $5V \pm 5\%$. An external voltage controls the output width by biasing IC_1 's negative input, but this option increases the circuit's sensitivity to power-supply variations. The minimum input trigger width is 2 nsec to maintain the programmed output width within 1%.

20-nsec-response overvoltage-protection circuit

You may often need to protect an expensive load from supply overvoltage. Overvoltage events may result from supply

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failure or poor transient response. In **Figure 12a**, Q_1 , a source follower, receives gate overdrive bias from the 12V bias supply that saturates Q_1 . The regulator driving Q_1 's drain takes feedback from the source and eliminates Q_1 's saturation resistance as an output-impedance term.

IC_1 monitors the 3V output that feeds the protected load. Under normal conditions, IC_1 's positive input is below its negative input, and its output is low. Q_2 through Q_5 are off, and the load receives drive via Q_1 . When an overvoltage event occurs, the 3V output rises. IC_1 detects this rise, and its output goes high. Q_2 and Q_3 come on quickly, pulling down Q_1 's gate. Q_4 and Q_5 , which are slower devices, turn on after Q_2 and Q_3 and shunt Q_1 's residual output to ground without experiencing excessive current. A 330V resistor feeds IC_1 's output to its latch pin, which causes IC_1 to latch high and prevents any output until the overvoltage cause is corrected. Breaking the latch with the NO reset switch resets the circuit.

The switching optimizes turn-off time (**Figure 12b**). Trace A is the 3V output, Trace B is IC_1 's output, and Trace C is Q_1 's gate. The output's amplitude (Trace A) excursion begins just before the second vertical division. IC_1 responds (Trace B) by going high, turning on Q_2 and Q_3 . This initial turn-on pulls Q_1 's gate downward, which Trace C shows, arresting the output's positive-going excursion in 20 nsec. As Q_2 pulls charge out of Q_1 , gate bias decays. When Q_4 and Q_5 come on, Q_1 is out of saturation, and the output drops rapidly. The circuit arrests the overvoltage event in 20 nsec and shuts down in 150 nsec. Bypassing Q_1 's source is optional; this option slows the overvoltage rise time but also restricts turn-off time. Similarly, the optional RC filter eliminates noise-induced nuisance tripping at the expense of response time. e

References

1. Williams, Jim, "High speed amplifier techniques," Linear Technology Corp, Application Note 47, August 1991.
2. Williams, Jim, "Practical circuitry for measurement and control problems," Linear Technology Corp, Application Note 61, August 1994.

Author's biography

Jim Williams is a staff scientist at Linear Technology Corp (Milpitas, CA), where he specializes in analog-circuit and instrumentation design. He has served in similar capacities at National Semiconductor, Arthur D Little, and the Instrumentation Laboratory at the Massachusetts Institute of Technology (Cambridge, MA). He attended Wayne State University (Detroit) and enjoys art, collecting antique scientific instruments, and restoring old Tektronix oscilloscopes.

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