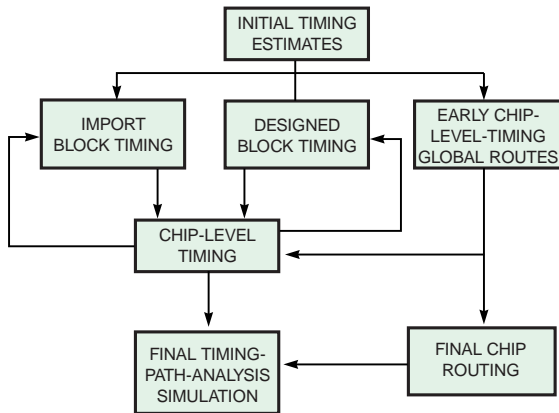


Figure 5



Complex core-based chip designs require a hierarchical timing flow in which you distribute your full-chip timing budget among individual cores and global interconnect.