

*****REGISTERS ADDRESSES
 DEFINITIONS*****

.EQU FLAGS,002FH
 .EQU BCOUNT,004FH
 .EQU CHANNEL,004DH
 .EQU VOLUME,004EH

*****INTERRUPT SUBROUTINE
 HANDLER*****

;THE NUMBER OF MACHINE CYCLES TO EXECUTE THE COMMAND ARE
 GIVEN AT THE ;RIGHT-HAND SIDE. THREE ADDITIONAL CYCLES ARE ADDED
 FOR THE RESPONSE TO ;THE INTERRUPT REQUEST

```
.ORG 006BH
      CLR IEN0.7; DISABLE ALL INTERRUPTS          1
      PUSH ACC;                                  2
      PUSH PSW;                                  2
      MOV A,BCOUNT;                               1
      JZ ALL_BY; TEST IF THE LAST BIT TO SEND    2 -> 8 + 3 = 11
      DEC A;                                       1
      MOV BCOUNT,A;                              1
      MOV A,CHANNEL;                              1
      RLC A;                                       1
      MOV P1.2,C; SEND THE BIT                    2 -> 14 + 3 = 17
      MOV CHANNEL,A;                              1
      SETB IEN0.7;                                1
      POP PSW;                                     2
      POP ACC;                                    2 -> 22 + 3 = 25
      RETI;                                        2
ALL_BY: MOV A,CHANNEL; THE LAST BIT TO SEND      1
      RLC A;                                       1
      MOV P1.2,C; SEND THE BIT                    2 -> 12 + 3 = 15
      CLR FLAGS.0; INFORM S16BIT FUNCTION         1
      POP PSW;                                     2
      POP ACC;                                     2
      ANL T2CON,#0ECH; STOP TIMER 2              2
      SETB IEN0.7; ENABLE INTERRUPTS             1
      RETI;                                       2 -> 22 + 3 = 25
```

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*****
;THIS COMMANDS SHOULD BE PLACED SOMEWHERE IN THE BEGINING OF
THE MAIN ;PROGRAMM
      MOV SP,#06H; SET THE STACK POINTER
      MOV IP0,#020H; SET THE INTERRUPT PRIORITY LEVEL OF CC3
      MOV FLAGS,#00H; CLEAR ALL BITS
      SETB IEN0.7; ENABLE ALL INTERRUPTS
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*****LM1972 INTERFACE CONTROLLING
 FUNCTION*****

```
S16BIT: MOV TL2,#(255 - 25);SET TIMER 2 COUNT REGISTER
      MOV TH2,#0FFH
      MOV CRCL,#(255 - 25);SET TIMER 2 RELOAD REGISTER
      MOV CRCH,#0FFH
      MOV CCL1,#0FCH; SET VALUE FOR CC1 - CLK SIGNAL
      MOV CCH1,#0FFH;
      MOV CCL3,#(255 - 25); SET THE BEGINING OF INTERRUPT
      MOV CCH3,#0FFH
      MOV BCOUNT,#07H; NUMBER OF BITS TO SEND - 1
      SETB FLAGS.0
      ANL P1,#070H; INITIATE PORT 1
      MOV CCEN,#088H; ENABLE COMPARE MODE FOR CC1 AND CC3
      SETB IEN1.5; ENABLE INTERRUPT FROM CC3
      ORL T2CON,#011H; START TIMER 2 WITH OVERLOAD ENABLED
S16_1: JB FLAGS.0,S16_1; WAIT UNTIL THE FIRST BYTE IS SEND
      MOV TL2,#(255 - 25); REINITIATE TIMER 2 COUNT REGISTER
      MOV TH2,#0FFH
      MOV BCOUNT,#07H; REINITIATE NUMBER OF BITS TO SEND
      MOV A,VOLUME; SWAP VOLUME AND CHANNEL CONTENTS
      MOV CHANNEL,A
      SETB FLAGS.0
      ORL T2CON,#011H; START TIMER 2 WITH OVERLOAD ENABLED
S16_2: JB FLAGS.0,S16_2; WAIT UNTIL THE SECOND BYTE IS SEND
      MOV CCEN,#00H; DISABLE CC1 AND CC3 UNITS
      CLR IEN1.5; DISABLE CC3 INTERRUPT
      ORL P1,#07H; SET OUTPUT PINS TO THE HIGH STATE
S_END:  RET
```

Figure 1. Listing of the assembler code for the digital potentiometer interface.