

Change partners and dance



Silicon-foundry and ASIC-vendor roles for chip design and fabrication are changing. If someone had asked me 10 years ago what a silicon foundry does, I would have said that the foundry processes silicon wafers for chip vendors that either have no silicon-processing capabilities or have an undercapacity problem at their own processing facilities. However, today's silicon foundries are taking on more of the tasks that ASIC companies traditionally handled.

In the mid-1980s, ASIC vendors offered a range of products and services for their customers, resulting in one-stop shopping for many companies. Designers went to ASIC companies for their expertise in designing leading-edge chips. ASIC customers often accessed this expertise through the services of geographically distributed design or technology centers in strategic places throughout the country or, in some cases, throughout the world. Besides having knowledge of high-complexity design methodologies, ASIC designers also had experience using the EDA tools needed to design high-density, high-speed chips.

Design tools came from ASIC and EDA-tool vendors, which counted ASIC companies among their best customers. ASIC and EDA vendors often worked closely to verify new EDA tools before the EDA vendor made these tools available to other customers. Along with some internally developed tools, the ASIC houses supplied cell libraries, covering both standard-cell and gate-array design implementations. Supplementing ASIC cell libraries were compilers for structured blocks, such as SRAMs, ROMs, and even datapaths. In addition, many ASIC companies also developed megacells, which were larger, more complex blocks of predefined and preverified logic that you could use on multiple designs. Megacells were the forerunner of today's intellectual-property (IP) cores. Rounding out this rather full set of offerings was state-of-the-art wafer processing at the ASIC vendor's facilities, followed by chip packaging and testing. Sili-

con foundries were just starting out and offered one product—silicon-wafer processing.

Fast-forward to the present, when the roles of ASIC vendors and silicon foundries have changed a lot. Third-party EDA tool and library vendors have eliminated design-tool and cell-library products from most ASIC companies. Foundries have forged partnerships with many EDA-tool, design-library, and IP vendors. These relationships allow such vendors to design their products for and verify their products on a process-by-process basis, a necessary consideration with deep-submicron complexity. Foundries have also become the place to go for some ASIC libraries and memory blocks (including DRAM and flash). Finally, a process-technology gap between ASIC companies and foundries is shrinking along with the process technology. One major foundry claims that by 1999, its most advanced process will be on par with that of a

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leading microprocessor company. So, what's left for the ASIC vendors? Plenty.

ASIC companies still offer important products and services for chip designers. ASIC vendors have a good understanding of deep-submicron-design methodology, because the vendors use this methodology for their own ASIC and standard-product chips. For both hard and soft IP cores, third-party vendors are excellent sources for common blocks, such as Universal Serial Bus and PCI cores, but the more complex nature and customer-specific attributes of DSP, microprocessor, and true ASIC cores mean you're probably better off getting these cores from an ASIC vendor.

As a designer, this change of vendor sources means that you win. You get your design tools, libraries, cores, and design methodology from companies specializing in these products and services. ASIC companies know how to design complex chips and have the high-end cores needed for these chips. Foundries have become good sources of well-verified silicon processing and have added ties to core and library vendors to make their products more robust. You're changing partners, but the dancing doesn't stop. In fact, the music is getting faster.

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Back to the breadboard



Once, a long time ago, logic design was straightforward. You wrote out your truth tables, drew your maps, worked out your Boolean equations, did a bit of minimisation, and pretty soon you were ready to reach for the orange book of MSI TTL functions. Before long, you had a rough cut of the function you wanted, soldered (or wire wrapped) together on the bench in front of you. An indeterminate amount of time later (the length of time often depending on how good you were with the fast oscilloscopes of the day), you had most of the bugs worked out of the design, and the next version of what usually turned out to be an extended family of prototypes was under way.

Then things started to get complicated. Designs became more and more complex, designers began to use simulation in a meaningful way, and methodology changed. The EDA business started to sell the concept that the whole design should be carried out in the "virtual" environment of the simulator, that there should be only a few prototypes (or even just one), and that the first specimen you built should be, for all practical purposes, identical with the first production unit.

Today, both ASIC and, albeit recently, FPGA vendors offer devices with very large gate counts that demand the importation of substantial blocks of intellectual property to fill them within a reasonable time. At the same time, new design methodologies struggle to keep up; gate-level simulation has faltered, faced with the scale of the full system simulations that replaced the old prototyping methods; and techniques such as cycle simulation and formal verification have come on rapidly to try to fill the gap.

Now, here's a curious thing: ASIC vendor VLSI Technology has introduced Velocity, a design flow that aims at addressing the shortcomings of today's tools when faced with today's development schedules. And what is a key element of this approach to cutting the design cycle? Hardware. As a cornerstone of Velocity, VLSI has built a library of bonded-out chips of its most used IP functions. At the same time, you can use the same standard buses on chip (PCI, for example) that you would use at the system level. There's a lot more to Velocity's approach than that; it is very much a language-based flow that appears to use the latest incremental synthesis techniques to optimise elements from the stock parts library to the precise feature mix that you want.

Still, this situation means you can check out major segments of your embryonic ASIC design by building them—and building them quickly. VLSI probably won't thank me for using the word, but

it looks a lot like the breadboard is back, which begs the question, did it ever really go away?

I don't think it did. Even in an era in which prototyping a complete system has become impractical, we still explore critical circuit functions in hardware. HP and Tektronix (and others) continue building better logic analysers; these analysers' uses are not confined to the system-integration phase. And one of the benefits of design reuse is that some of the confidence you get from having hardware working on the bench you inherit with the reused elements. Also, I suspect that, in more organisations than might care to admit it, there's still an element in management that looks over your shoulder and says, "Yes, I'm sure the simulation is running beautifully, but don't you have something you can *show me*?"

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