

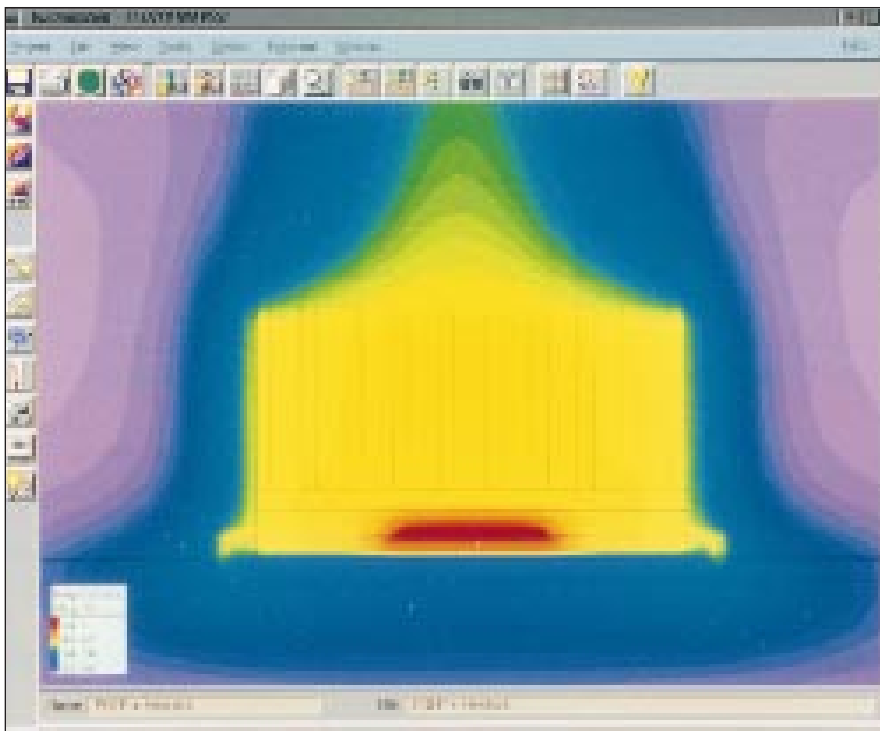


## Automatic features simplify thermal analyses

Version 2 of Flomerics' Flotherm thermal-analysis package now runs on Windows NT or Unix. Version 2 includes a rewritten user interface, giving the package the look and feel of typical Windows-based EDA and CAD software. Using the package, you can create, edit, and manipulate graphics in a CAD-style environment, using three primary application windows. A project-management window shows the model's hierarchy and gives an improved sense of the structure of the model and the source of data for its various components. In the drawing-board window, you can create geometry with the mouse, as with a CAD package, and in the visualisation window, you use OpenGL graphics techniques to provide a comprehensive view of the model with zoom, pan, rotate, and walk-through effects.

Flomotion, one of Flomerics' new modules, operates in the visualisation window; it lets you project the image of airflow around components in a complex model. The module adds coloured "particles" to the view and moves into successive frames to give an impression of the air's movement. Colours represent the temperature of the moving air. This approach, says Flomerics' Mike Reynell, gives an instant impression of heat-flow details that you might glean only after considerable time studying temperature profile "stills." Version 2 also allows you to parametrically model common electronic-system components, such as fans, heat sinks, and pc boards, by giving dimensions to standard parts.

The latest addition is a routine to import geometric data directly from mechanical CAD packages that design the physical components of a system. Importing data from packages such as AutoCAD sounds fairly trivial, Reynell acknowledges, but the challenge is in data reduction. CAD files contain a wealth of data on mechanical details of parts, much of which is irrelevant to a thermal analysis. Embodying a rule set into



A detailed analysis of heat-sink performance yields surprising results.

Flo/MCAD to reduce the data to a set that will yield a reasonable size of mesh for the fluid-dynamics analysis is at the heart of the module's operation. You can observe and control the simplifications of the MCAD data or let the software do it; it automatically decomposes each part into Flotherm primitives.

Feedback from users indicates that use of thermal analysis often yields valuable insights into effects that go against intuition; Reynell cites an analysis of a finned heat sink on a PQFP. Without forced airflow over the fins, the dominant effect of the heat sink was to conduct heat from the silicon die, up through the package plastic, out to the edge of the package, back through the plastic, and down through the package pins to the pc board. Under pure convection (no fan), the finned heat sink was little more effective than a flat plate placed on top of the package.—by Graham Prophet

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## Build a CPU-hosted USB modem with two-chip set

With STMicroelectronics' Pegas.usB chip set, you can design a V.90 modem that connects directly to a Universal Serial Bus (USB) port. The two-chip set encompasses the ST7554 USB world-modem controller and STLC7550 modem analogue front end. It uses TQFP and runs at 50 mA in operating mode and 500  $\mu$ A in suspend mode, so the USB power line can provide power. Price is \$30 (10,000). The chips use the USB-Modio from Smart



USB modems will be installation-free and plug-and-play on Windows 98.

Link host-based modem techniques running the DSP functions on a PC's main processor. With a recommended minimum of a 200-MHz Pentium, the overhead is "barely detectable," STM says. The chip set is also ready for the V.80 video-phone standard and has automatic identification and fallback to earlier standards. Next year will see STM extend the family to include a transformerless data-access-arrangement version and one with voice speakerphone and cellular support.

You can get designs under way with an evaluation package that includes a USB "dongle"-style modem and software with full reference-design data.

—by Graham Prophet

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## Adjustment-free designs target UHF radio links

A transmitter/receiver IC pair, the CMX 017 and 018 from Consumer Microcircuits, operates across the 865- to 965-MHz band and is suitable for use in a variety of fixed-frequency or spread-spectrum radio links using FM/FSK modulation. You can run both parts from 2.7V. The transmitter incorporates an RF VCO modulator and power amplifier, which delivers 20 dBm (100 mW) to either drive a power-amplifier stage or connect directly to an antenna for handset use. A buffered local-oscillator output provides RF to an external synthesiser or PLL for channel selection, and the pair provides gain control over a 20-dB range of the power-amplifier driver stage. You can control power by individually switching off the power amplifier and driver (transmit standby) while powering the rest of the circuitry for frequency stability or by shutting down the whole device. Consumer Microcircuits says that the modulator supports data rates of 384 kbps in

## DILBERT® by Scott Adams





digital mode. You need not choose from a frequency-banding selection; one chip covers the entire frequency range. Off-chip base-band modulators can feed the same RF stage for more complex modulation modes.

The 018 receiver is a conventional double-conversion superheterodyne design with a dual-mode low-noise amplifier; two downconverters, including integrated oscillators; limiting amplifiers; a received-signal-strength indicator; an FM/FSK demodulator; and power control. Its design-

ers note that some single-chip designs are less selective and sensitive than they could be; you must make a trade-off between performance and power consumption. The 018 uses more power than some devices (50 mA from 2.7V), but this consumption yields a high-quality low-noise amplifier and high-performance mixers that give good overload performance and good out-of-band rejection. In the crowded UHF band with low-power services operating alongside strong adjacent signals, good sensitivity and dynamic range are

essential. You need only one SAW ahead of the receiver's low-noise amplifier rather than a highly selective filter; a 70-MHz first IF keeps image responses out of the way, and the second IF uses standard 10.7-MHz, broadcast-type filters for low cost. As a result, you can expect to design a board free of final-adjustment problems.

—by Graham Prophet

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## Visualise your product early for concurrent engineering gains

Version 4.5 of Rapid Plus, a development tool for system man-machine-interface development, adds the ability to generate code that you can use in production versions of a design. Emultek wrote the original Rapid, a simulation and modelling package for man-machine interfaces. With the package, you model a proposed design in terms of the front-panel objects—and their expected behaviour—that the eventual user will see. The principle is process simulation rather than using a formal specification language. Marketing and engineering departments can, say the system's developers, come to an agreement on how the product should respond, and then embody this response in an executable form. The representation is state-diagram-based, and you define the model in terms of modes of response and the actions to get from one mode to the next. You can then use Rapid Plus for a variety of concurrent engineering tasks, such as test generation, documentation, training, marketing,

sales-tool development, and code generation.

The software outputs C code for the man-machine interface, and a Rapid kernel runs on a variety of target  $\mu$ Ps with links to popular real-time OSs. Emultek estimates that the overhead for using hand-crafted code is no more than 10 to 15% in a project of 100,000 lines of code. You can use a customised interface layer between the Rapid code running the man-machine interface and the remainder of the embedded-system software. This system outputs state diagrams; design occurs at a higher hierarchical level, according to Westland System Assessment, the UK agent for Emultek. The company also notes that it will keep code size in line with design complexity and that the Rapid environment can handle concurrent modes.

Westland is also the UK source of the Care software package from BQR Reliability Engineering. Care forecasts the reliability and maintainability of a product on an analytical and statistical basis. Intend-

ed as a design tool for hardware engineers and test engineers, it can access a variety of CAD and EDA database formats and has links to simulation tools, including Spice. It forecasts MTBF and component stress and, if a thermal-analysis package is lacking, performs a first-order thermal analysis to predict device temperatures. It includes modules for reliability planning; testability analysis; and whole-life product management, including scheduling maintenance and providing spares. By providing a means of whole-life costs, it lets you address increasingly important design-for-end-of-life issues.

—by Graham Prophet

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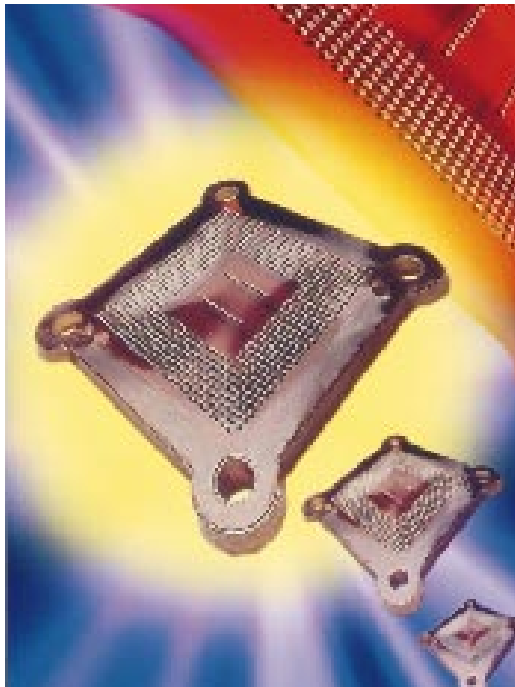
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## Chip I/O densities continue to rise

Until now, designers have associated chip-scale packaging and formats such as  $\mu$ BGA with high-pin-count devices; now, Xicor has created the Xicor BGA (XBGA), which packages die with as few as eight pins. EEPROMs packaged in this technology have a footprint essentially the same as that of the die. The assembly procedure for the package starts with a thin glass wafer, which the manufacturer bonds to the front of the die. Xicor then laps down the silicon wafer to reduce its thickness, a standard operation for low-profile packages, separating the die by etching rather than sawing. The company then bonds a second glass wafer to sandwich the silicon, cuts the front-side glass layer to expose the aluminium connections of the die, deposits more aluminium to bring the connections to the top of the front-glass layer, and then applies solder bumps to that layer. Xicor then separates the die; sealing is inherent in the process, and the process uses no epoxy overmould. You can buy 64- and 128-kbit EEPROMs in the 0.5-mm-thick package for \$1.70 to \$2.95 (10,000), depending on density and serial interface.

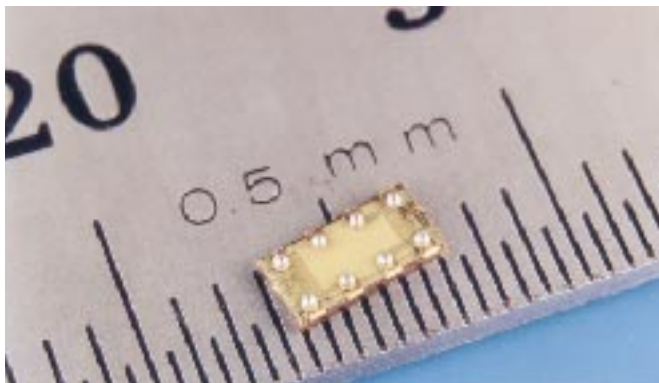
Last year, Toshiba and Fujitsu introduced a BGA multichip package that placed flash and SRAM die side by side in one package measuring about 1 cm per side, which the two companies say has found good acceptance in cellular-phone designs. As a derivative of that technology and with the added participation of NEC, the companies are defining a new format that will stack the two die to further reduce footprint. The two die are one NOR-type 4- to 128-Mbit flash and one 1- to 16-Mbit SRAM in various combinations. The format defines an  $8 \times 8$ -ball layout on a 0.8-mm pitch using 56 positions; the format is pin-compatible with all combinations of



Serial EEPROMs now come in packages only fractionally larger than the die (courtesy Thomas and Betts).

memory, and a pin provides switching between  $\times 8$  and  $\times 16$  outputs. The format requires 70% less area than two TSOPs. Samsung, Seiko Epson, and Hyundai also support the format, and samples should be available by year-end.

IBM has also announced new formats for high-integration ASICs and systems. The company uses ultra-fine-pitch wire-bond plastic BGAs to reduce die pitches to less than 60  $\mu\text{m}$  for high-



Make reliable contact to large-pin-count packages without damaging pressure (courtesy Xicor).

er I/O counts and densities of more than 1000 I/Os. A second technique, glass-ceramic chip carrier, addresses footprint, thermal, and electrical issues; it eliminates thin films from the glass ceramic for cost reasons and, by matching substrate and silicon thermal characteristics, handles very large die for 5000 interconnects on the package and more than 1600 connections off the package. The technique uses the C4 flip-chip die-attachment technology. IBM is also employing a multichip-module (MCM) technology that uses a laminate substrate, providing MCMs' usual density and performance gains and controlling costs.

And, how do you connect your very-high-pin-count IC to a board if you want a removable device? Thomas and Betts offers a new interconnection system for that need. The company based the system on metallised particles embedded in polymer. The system allows you to connect packages with more than 1000 I/Os. Metallised-particle interconnect shapes the metal particles into tiny columns within a flexible polymer carrier in the socket. The technique achieves reliable connection at a force of 50 gm per contact, managing the forces for a complete, very large device. The system provides 1000 mating cycles and 0.2-nH mutual inductance between columns.

—by Graham Prophet

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