

# Digital sync-tip clamping: a new approach to video-signal conditioning

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In digital sync-tip clamping, a stand-alone “clamping” ADC (CADC) incorporates the dc-restore function at its input and eliminates the need for external timing strobes. This technique encompasses a complete front-end architecture, including sync detection and automatic gain control (AGC) and provides more system-design flexibility in video applications than conventional ADCs. This CADC architecture is a promising configuration for a single-chip video-conditioning front end.

The two main advantages of digital sync-tip clamping are high accuracy and asynchronous operation. In other words, with a CADC, you don't need to recover the horizontal timing of the analog video. This feature simplifies the design if the application specifies a  $4F_{sc}$  sampling rate, such as in comb filters, or uses a free-running sample clock. (The  $F_{sc}$ , or sub-carrier frequency, for NTSC video is 3.58 MHz.)

With a conventional back-porch clamp, dc restoration, or clamping, must occur before you set the signal level at the ADC's input. However, to digitally extract timing-control signals, the circuit needs to first define either the sync-tip or the back-porch reference-voltage levels. To break this “loop,” the circuit must initialize the digital timing with an auxiliary analog separator. The CADC avoids this problem. Because the digitized video has a fixed dc level, you can directly obtain the sync information and the AGC's error signal from the digital data.

## Video front end needs clamping

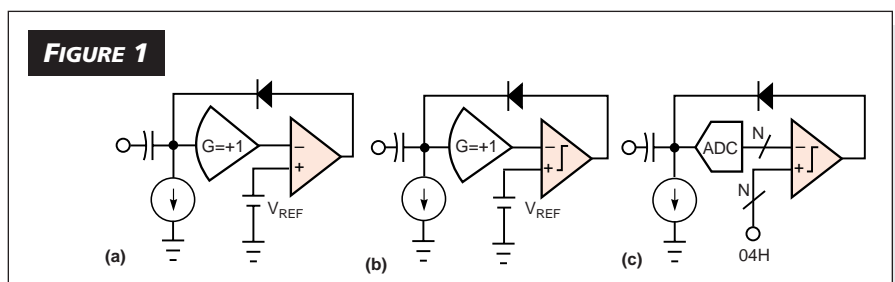
To digitize an ac-coupled video waveform, dc restoration is necessary to put a dc component back into the video signal. Usually, some type of switchable device, such as an analog switch, operational transconductance

Digital sync-tip clamping allows an ac-coupled ADC to digitize analog video without restoring the horizontal timing. You can implement the technique as a stand-alone clamping ADC or as a complete front-end configuration, including sync detection and AGC.

amplifier (OTA), or S/H amplifier, performs the dc restoration function. The circuitry adjusts the clamp level to the chosen value during the back-porch section of the video signal. Then, the circuitry stores this value during the active-line time. It is important to set the clamp level during a

specific line interval because the circuit needs to recover the horizontal timing information before clamping. In other words, the circuit must recover the information from the ac-coupled signal.

Another dc-restoration method based on sync-tip clamping uses no temporal information. This essentially analog technique is subject to temperature dependencies and part tolerances; therefore, it is too precise for dc restoration. However, designers often use this technique for sync detection. **Figure 1a** shows the sync-tip clamp used in such ICs as the industry-standard LM1881 (National Semiconductor, [www.nsc.com](http://www.nsc.com)), the EL4581/83 (Elantec, [www.elantec.com](http://www.elantec.com)), the GS4881 and GS4991 (Gennum Corp, [www.gennum.com](http://www.gennum.com)), and others. This circuitry clamps the negative-going sync tip to the  $V_{REF}$  voltage. A unity-gain buffer outputs the clamped video.



Sync-tip clamping using either an op amp (a) or a comparator (b) is a common technique for sync detection. Digital sync-tip clamping (c) embeds an ac-coupled ADC in the clamping feedback loop, a scheme that performs dc restoration without horizontal-timing information.

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You can use an alternative clamp configuration for coarse dc restoration. In this configuration, the clamping circuit uses a simple analog comparator that feeds positive current back to the buffer's input when the buffer's output is more negative than the clamp reference voltage (**Figure 1b**). The GB4550 and GB4570 (Gennum Corp) video buffers/clamps use this configuration. There is no meaningful difference between the configurations in **Figure 1a** and **Figure 1b**. In both cases, the performance of the error-detection scheme limits the clamping accuracy.

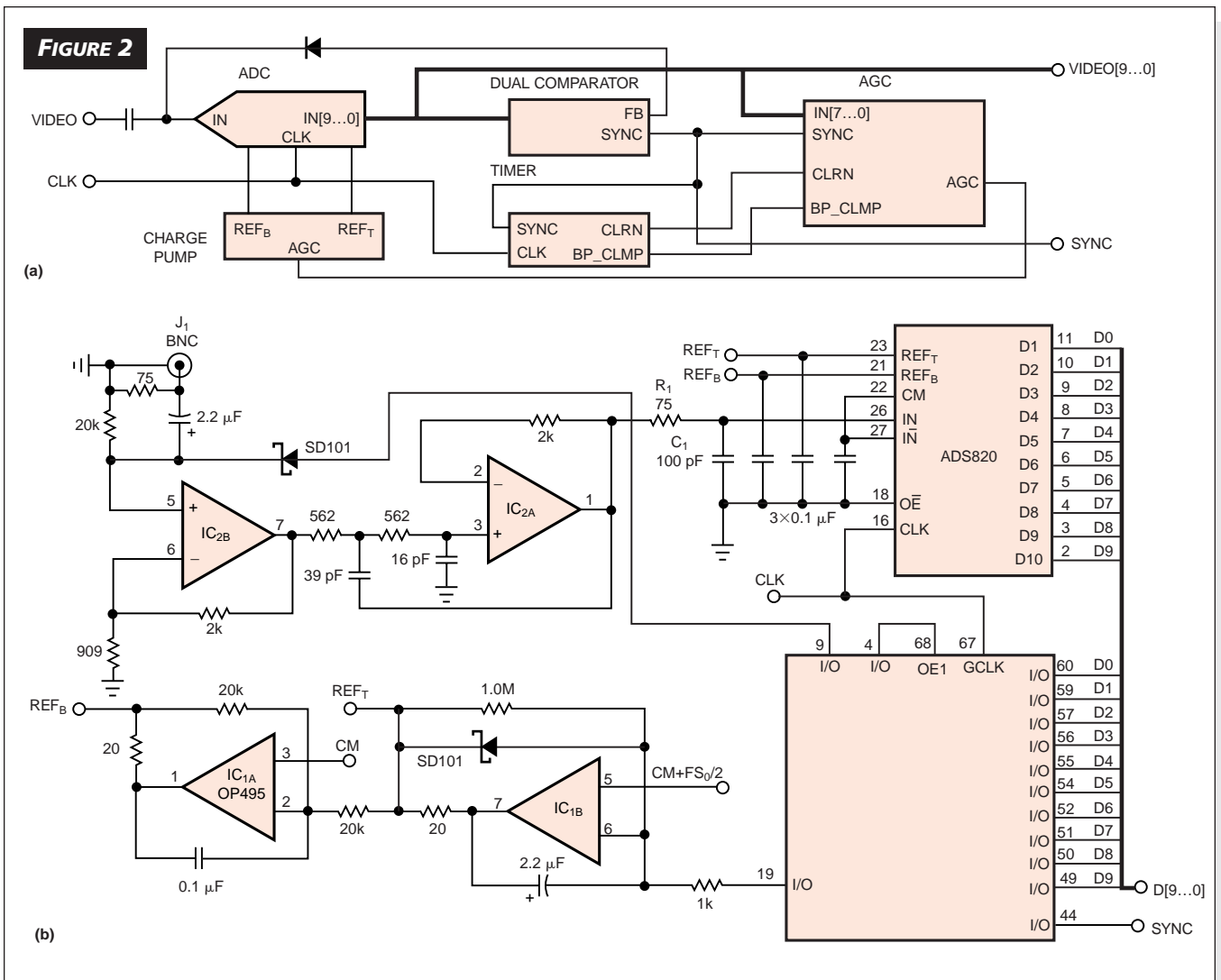
Unlike known dc-restoration methods, digital sync-tip clamping doesn't require dc-restored signals to drive the ADC. Instead, it embeds an ac-coupled converter into the clamping feedback loop (**Figure 1c**). The CADC comprises a conventional converter, an N-bit digital comparator, a clamping diode, a current sink, and an ac coupling capacitor. Basically, a digital comparator and a feedback loop that

embraces the overall signal-processing chain achieve high-precision clamping.

How the CADC works

The CADC is a negative-feedback system (**Figure 1c**). The output variable, which is the digitized video, drives the inverting input of the comparator. The noninverting input connects to the nominal sync-tip level (4 LSB for an 8-bit system). The comparator output delivers the error-correcting signal to the ADC input. Thus, the proposed CADC consists of single-loop analog-to-digital conversion and clamping.

To understand the circuit's operation, assume first that no input signal exists. If the ADC's output data is less than the nominal reference level, the comparator's output state is high. In this case, the capacitor charges through a forward-biased diode. When the output code crosses the reference level, the comparator switches to a low state and blocks the



The major elements of the video-conditioning front end include the ADC itself, a charge pump, an AGC controller, dual digital comparators, and a timer (a). A sample design incorporates all digital functions into an FPGA (IC<sub>1</sub>) (b).

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diode. The ac-coupling capacitor then acts as a hold device and discharges slowly through the current sink.

The comparator output switches back to high when the voltage across the capacitor drops even 1 LSB below the reference level. The held voltage across the coupling capacitor fluctuates around an arbitrary value of  $V_0$ , which causes the output digital data to vary from 3 to 4 LSBs, regardless of temperature drift and part tolerance.

This ripple is inherent for a two-position, on-off control. Essentially,  $V_0$  settles to a value that ensures a balance between the average current that the comparator supplies and the current sink that discharges the capacitor. Because the charge current ( $I_c$ ), is much greater than the sink current ( $I_s$ ), you can express the approximate ripple period as follows:

$$T_{\text{RIPPLE}} @ \frac{C \cdot FS}{I_s \cdot N},$$

where  $C$  is the value of the coupling capacitor, and  $FS$  and  $N$  are the ADC input's full-scale range and bit number, respectively. Because the switching duty factor of  $I_s/I_c \ll 1$ , the output code has a nominal value of 4 LSB during most of the self-oscillation period; otherwise, it drops to 3 LSB.

### Add the video input

Now consider what happens when you apply a video signal to a circuit that has been operating in this stand-alone, no-input mode. The first sync pulse causes a transient current to flow through the capacitor. The ADC input instantly drops below  $V_0$ , which forces the comparator to switch to the high state. Accordingly, the capacitor acquires the error-correcting current, and the voltage across the capacitor increases to compensate the negative voltage step,  $V_s$ , induced by the sync pulse's leading edge.

On the trailing edge of the sync pulse, the input voltage rapidly becomes a positive-going signal, the comparator output goes low, and the capacitor discharges slowly through the current sink. For subsequent sync pulses, the capacitor's hold voltage varies, depending on the charge balance that the circuit established during the previous video line.

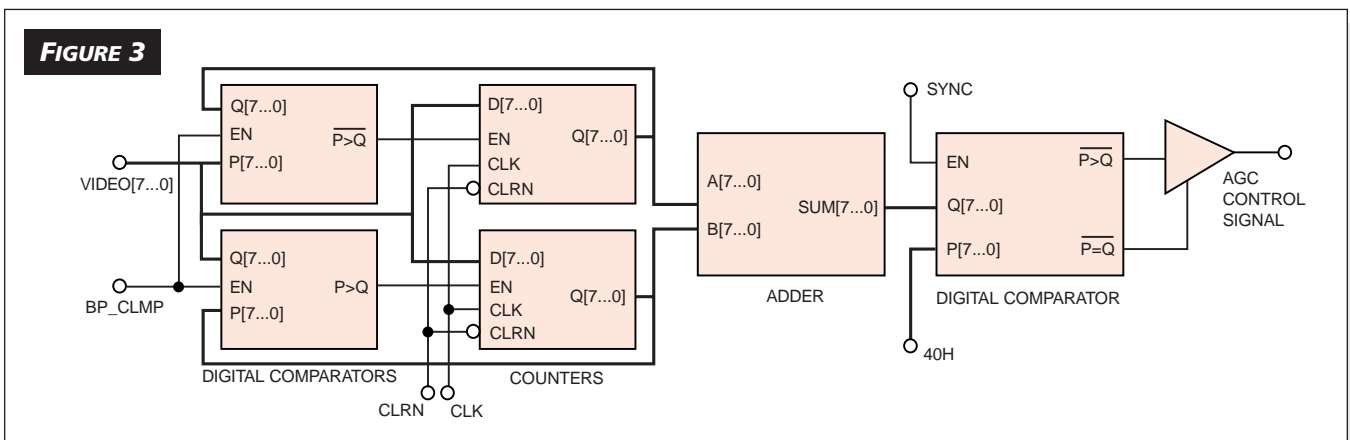
Under equilibrium conditions, the comparator supplies an average current that is just sufficient to balance the current that discharges the capacitor. In this case, the average voltage across the capacitor approaches a stationary level of  $V_1$ , where  $V_1 = V_0 + V_s$ . In other words, all signal variations take place at a voltage higher than the nominal sync-tip level. An on-off controller causes a 1-LSB p-p ripple of the clamping level. However, by choosing  $T_{\text{RIPPLE}} > 1/H$ , where  $H$  is the horizontal scan rate, the expected conversion error of 1 LSB occurs outside the active line's scan interval.

A block diagram of the proposed video front end integrates three digital modules with the ADC: a dual comparator, a timer, and an AGC controller (Figure 2a). One of the comparators supports the previously described clamp action. The second comparator defines the midpoint of the sync pulse's falling edge in the same manner as an analog sync stripper. The AGC controller generates an error signal, which drives the charge pump. The charge pump implements the error correction for the AGC loop.

### AGC loop makes adjustments

The AGC loop adjusts the ADC's full-scale range. For video applications, this adjustment is necessary because the amplitude can commonly vary by a factor of 0.5 to 2. In most cases, an AGC circuit determines the error signal by calculating the difference between the obtained and specified sync-height values. The circuit adjusts the entire video signal or reference voltage according to this error-signal value. No one method is the best for all instances. However, controlling the reference voltage of the ADC works best in most situations. The disadvantage of this method is that the AGC control range can't exceed the reference voltage margins allowed by the ADC's specification.

Most single power-supply ADCs have a pipelined and fully differential architecture. In this case, the top ( $REF_T$ ) and bottom ( $REF_B$ ) reference voltages center around the common-mode potential. Thus, for the single-ended input, the full-scale range is  $2 \times (REF_T - REF_B)$ , and the common-mode value centers at  $(REF_T + REF_B)/2$ .



The digital AGC controller includes two peak-detectors, which consist of comparators and counters, an adder, and another comparator.

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When designing an AGC circuit, the expected range of dc voltages at the ADC's reference inputs corresponds to a desired full-scale conversion range. In practice, the controllable reference (REF) varies from a minimum ( $REF_{MIN}$ ) to a maximum ( $REF_{MAX}$ ). You can adjust the reference voltage, but you must keep the ADC's common-mode voltage fixed. A sample circuit meets these requirements and incorporates all digital functions in an EPM7096LC68 FPGA (Altera Corp, www.altera.com) (**Figure 2b**).

### Design the ADC's analog interface

The analog portion of the circuit in **Figure 2b** configures op amp  $IC_{1B}$  as a charge pump, which delivers the top reference voltage,  $REF_T$ . Assume that the noninverting node of  $IC_{1B}$  connects to a voltage source equal to  $CM+FS_0/2$ , where  $FS_0$  is the desired full-scale range at power-up when the AGC has no effect and where  $CM$  is the common-mode value. In this case, you can express the top reference voltage as  $REF_T = CM+FS_0/2+ERR$ , where  $ERR$  is the error-correcting signal.

$IC_{1A}$ 's unity-gain inverter drives the bottom reference voltage,  $REF_B$ . Because  $IC_{1A}$ 's noninverting input connects to a voltage source equal to common mode,  $IC_{1A}$ 's output yields  $REF_B = CM-FS_0/2-ERR$ . Thus, the controllable reference-voltage range becomes  $REF = REF_T - REF_B = FS_0 + 2ERR$ .

The expected AGC range should match the ADC's specification. For the ADS7850 ADC, this requirement means that  $REF_{MIN}$  should be greater than 0.8V dc. Similarly,  $REF_{MAX}$  should be less than 2.3V dc. Therefore, the ADC's full-scale input range is limited to 1.6V p-p <  $FS < 4.6V$  p-p. Implementing the input buffer with the gain of 3.2 ( $IC_{2B}$ ), this front end accommodates -6-dB to +3-dB variations from the nominal 1V p-p full scale.

Regarding specific dc levels, it is suitable to choose  $FS_0 = REF_{MIN}$ . Because this input range is the lowest allowable, you can assume that  $ERR > 0$ . In this case, you can use  $D_1$  to ensure that  $REF_T > CM$  regardless of potential ringing during transitions. The ADC's specifications give the common-mode value.

Because the circuit sets the clamping level according to  $REF_B$ , the AGC operation may affect the clamp operation. You can avoid any interaction by making the time constant of the AGC loop much greater than the settling time of the second

loop. In this case, the clamping loop sees the bottom reference voltage as a fixed value.

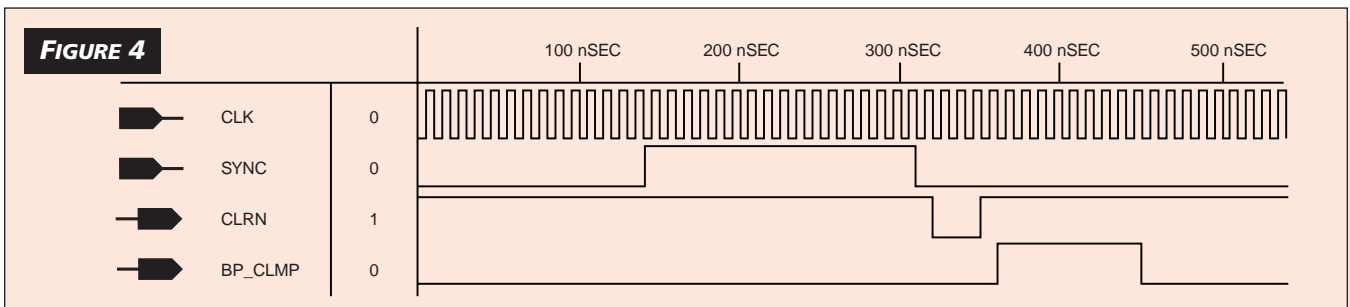
**Figure 2b**'s circuit also includes a unity-gain, third-order, antialiasing circuit, which comprises a cascaded, second-order, active lowpass filter ( $IC_{2A}$ ), and a first-order passive filter ( $R_1/C_1$ ).

### CADC doesn't use digital filtering

The AGC operates by estimating the difference between the obtained and specified sync height. Once the sync tip is fixed, the circuit must sample the back porch to determine the digital blanking level. Because this action requires removing subcarrier information, the composite video signal requires digital filtering.

Unlike common processing schemes, this CADC doesn't use a digital lowpass filter to reject the high-frequency components. Instead, the scheme defines the blanking level as  $(CB_{MIN} + CB_{MAX})/2$ , where  $CB_{MIN}$  and  $CB_{MAX}$  are the minimum and maximum samples from the burst envelope. The algorithm implementation is straightforward and includes two peak detectors (comparators and counters), an adder, and another comparator (**Figure 3**). The peak detectors compare the current digital value with the delayed one. To detect the maximum sample, the circuit enables the register for writing. When the value of a new entry exceeds that of the previous entry, the comparator output switches the register to the hold state. Hence, the register contents represent the most recently obtained maximal sample. The minimum detecting scheme is identical. The peak detectors, which are active only during the BP\_CLMP interval, deliver the required  $CB_{MIN}$  and  $CB_{MAX}$  values.

Asynchronous sampling of the color burst potentially causes artifacts. Because of the effect of interference on the digitized sine wave and sample clock, sampling occurs at an arbitrary phase. Thus, the digitized data exhibits line-to-line alterations. As a result, the blanking-level estimation varies periodically. However, because these variations are cyclic, a narrowband AGC loop effectively averages the error-correcting signals. This filtering ensures that the AGC's performance using minimum/maximum detection matches the system's performance using a digital lowpass filter. This approach also significantly reduces the gate count and simplifies the design. Synchronous sampling eliminates the artifact.



The SYNC, CLRN, and BP\_CLMP logical signals control the AGC operation. The BP\_CLMP gating interval points to the position of a color burst, and the circuit detects the maximum and minimum levels of the burst envelope. The circuit then applies the error-correcting signal to the AGC charge pump during the SYNC interval that follows.

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The SYNC, BP\_CLMP, and CLRN logical signals control the AGC circuit's operation. Threshold separation generates the SYNC signal from digitized video. Nominally, the threshold level is 16 LSB. Thus, for the minimum input level of -6 dB, slicing occurs at approximately 50% of sync-tip amplitude. When the circuit obtains the SYNC signal, this signal enables the timer that generates the BP\_CLMP and CLRN waveforms (Figure 4).

The BP\_CLMP gating signal points to the position of a color burst. You use this interval during operation to detect maximum and minimum levels of the burst envelope. You need not generate BP\_CLMP exactly as the horizontal-timing specification requires. Instead, BP\_CLMP has to encompass only the color burst. The trailing edge of SYNC asserts the CLRN signal, and BP\_CLMP clears the CLRN signal. This CLRN pulse provides system reset. The circuit processes all of the data on the horizontal line and then applies the error-correcting signal to the charge pump during the SYNC period.

Because the circuit internally generates the BP\_CLMP and CLRN intervals, the circuit needs to reference the timing of these intervals to SYNC. A sequence of two operations accomplishes this task. During the first operation, SYNC sets an up/down 8-bit counter for count-up. The trailing edge of SYNC initiates the second step. The circuit stores the obtained number of counts, N, and sets the counter for countdown. When the counter reaches zero in the count-

down mode, the circuit inhibits further counting.

The circuit generates an internal back-porch interval with an overall duration equal to SYNC. To select a given point within this interval, compare the number of counts with an adequate fraction of N. The sample design initiates the BP\_CLMP signal at  $3N/4$  and deasserts this signal at  $N/4$  counts. The timing simulation in Figure 4 illustrates this case when  $N=18$ . EDN

### Reference

1. Invention disclosure document No. 428721; patent is pending.

### Author's biography

*Lazar Shifrin is the owner of Advanced Imaging Solutions (San Jose, CA, www.pixeldata.com), a consulting and contracting service that specializes in real-time image and video processing. He holds an MSEE and a PhD in image processing from St Petersburg Electrical Engineering University (Russia). You can reach him at lshifrin@pixeldata.com.*

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