

Figure 2



By analyzing code-coverage results on different pieces of your chip, you can find where “holes” exist in simulation coverage and focus your efforts on increasing design testability. In this HDLScore example, instance MUX1 in module `fifo_tb.FIFO_INST` has 100% block and path coverage but only 85% expression coverage (indicated by “ok ok 85” in the center of the figure next to `fifo_tb.FIFO_INST.MUX1`). The bottom of this photograph indicates the cumulative coverage of module `fifo_tb.FIFO_INST` as 89% block, 85% path, and 83% expression.