

# EDN LEADING EDGE

WHAT'S HOT IN THE DESIGN COMMUNITY

EDITED BY FRAN GRANVILLE

## Fall brings a flurry of processors

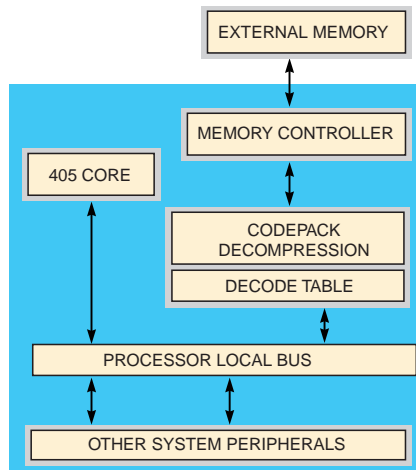
Fall has arrived, and with it comes the announcements of new processors and processor architectures. At the Microprocessor Forum in San Jose last week, ARM, BOPS Inc, Hitachi ([www.halsp.hitachi.com](http://www.halsp.hitachi.com)), IBM, Lucent, Motorola, QED ([www.qedinc.com](http://www.qedinc.com)), Rise Technology ([www.rise.com](http://www.rise.com)), Siemens ([www.sci.siemens.com](http://www.sci.siemens.com)), and Triscend ([www.triscend.com](http://www.triscend.com)) are but a sampling of the many companies introducing processors.

IBM's new PowerPC 405 core blows the doors off the company's 401. A pipeline increase from four to five stages allows the 405 to run at 200 MHz, and it can access two instructions per cycle into the fetch queue. It can simultaneously decode both instructions and examine branches one cycle before they happen; this technique allows the 405 to achieve a zero-cycle branch penalty using static-branch prediction. The 405's cache arrays are nonblocking to allow the core to overlap execution of instructions while line fills are in progress.

The 405 adds support for an auxiliary-processor-unit (APU) interface that allows IBM to tie customized execution units, such as a floating-point unit, a single-instruction multiple-data (SIMD) unit, or a DSP, directly into the processor's pipeline. The APU interface allows you to perform loads and stores directly to the APU's separate register file from the core. The APU has visibility into the low-level operation of the core's pipeline, including the decode stage. User-defined instructions can control the APU; the APU monitors instructions in the decode stage and prevents the core from

generating a fault on unknown instructions. The APU can run in parallel with the core but generates an interlock condition if a dependency between the two exists.

The 405 comes with a multiply-accumulate (MAC) APU, which adds nine operations to the standard instruction set. MAC instructions operate on either signed or unsigned 16-bit operands and accumulate the results in a 32-bit, general-purpose



The 405's optional codepack decompression core targets 60% smaller code and has no impact on the software environment.

register. Instructions can be unsigned, signed, modulo, or saturate.

The 405 has a CodePack decompression core that reduces an application's code size. Although CodePack is optional, IBM tightly wove its functionality into the code-fetch stream. IBM uses the MMU to designate which portions of system memory use code compression. Decompression uses a look-up table, and a variable-length encoding technique

occurs between memory and the instruction cache. When a cache miss occurs, the CodePack core decompresses code on the fly. Although IBM estimates that CodePack will deliver a 60% reduction in code size, there is a 10% latency penalty associated with the decompression process. Furthermore, CodePack consumes approximately 1 mm<sup>2</sup>, increasing the CPU-core size by roughly 50%. But on the positive side, CodePack has no impact on the software environment, unlike other code-compression techniques.

Faster ARM, new instructions

ARM detailed its new ARM10 family, which comprises the ARM10TDMI integer core, the VFP10 vector-floating-point coprocessor, and the ARM1020T cached integer core. The ARM10 is about 40% faster at the same frequency than the ARM9. But ARM targets the ARM10 to operate at 300 MHz, well above the maximum frequency of 200 MHz for ARM9.

When ARM invented the Thumb architecture, the company expected that programmers would stay in either ARM or Thumb mode, but programmers frequently jump back and forth between the two modes, which impacts performance. To remove that bottleneck, the new processor incorporates ARM's Version 5 instruction set for ARM and Thumb. Version 5 includes a branch-link-exchange instruction that performs a subroutine call and switches instruction sets in one operation. A new subroutine-return instruction, using a "load-multiple" instruction allows you to return to the instruction set (ARM or Thumb) that called the function, instead of manually switching modes.

Other new instructions include a "count-leading zeros" (CLZ), which is useful for graphics and encryption algorithms. CLZ provides the normalization part of the Newton Raphson reciprocal-approximation algorithm to improve integer-divide performance. Hence, ARM10TDMI performs an integer divide in one cycle per bit of divisor, compared with three cycles for ARM9.

From an architectural perspective, ARM10TDMI has a leg up on ARM9. Although both have a five-stage pipeline, the ARM10TDMI's pipe is much wider. In other words, ARM10TDMI is a single-instruction-issue machine, but it can issue instructions to its multiple functional units: ALU, branch unit, 32x16-bit multiply unit, load/store unit, and coprocessor unit. Each unit can work on a separate instruction in parallel, which comes in handy for some multicycle instructions.

The branch unit (BU) allows ARM10TDMI to achieve zero-cycle branches (three cycles worst case). Using static-branch prediction, the BU fetches code ahead of the core. The BU optimizes branch instructions by fetching instructions ahead of the core, calculating the branch-target address, loading the instruction from that address, and passing this instruction to the core instead of the branch. The ARM10TDMI also

supports a nonblocking, hit-under-miss data cache that allows the core to execute instructions that don't require the missing data after a cache miss.

The VFP10 coprocessor connects to the ARM10TDMI via a dedicated coprocessor interface that comprises two unidirectional, 64-bit buses. On the ARM7 and ARM9, the coprocessor hangs directly off the main CPU bus, causing loading that limits clock rates. The VFP10 has its own register file and supports single- and double-precision arithmetic; vector instructions; and multiply-add, compares, conversions, and other floating-point instructions.

The ARM1020T cached integer core contains 32-kbyte, 64-bit-wide, 64-way set-associative instruction and data caches. For design flexibility and to minimize power consumption, ARM built these caches from 4-kbyte blocks. ARM's cache-tag scheme allows the processors to determine the cache address and power up only one 4-kbyte block at a time. The ARM1020T also includes an MMU with demand-paged virtual-memory support and, therefore, satisfies the needs of Windows CE. The core supports a 64-bit-wide version of the Advanced Microprocessor Bus Architecture (AMBA) and handles split transactions, as does the PCI bus.

BOPS picks up the tempo

The BOPS ManArray is a general-purpose array-processor core with an encapsulated-very-long-instruction-word (eVLIW) architecture supporting 8- and 16-bit packed-data and 32-bit, single-precision, floating-point formats (see "EDN's 1998 DSP Directory," April 23, 1998, pg 50). The first incarnation of a ManArray core will use a five-instruction VLIW; each can execute in parallel. The core can conditionally execute each instruction, helping to minimize the use of branches in a program. The architecture supports both floating- and fixed-point operations that execute in two and one cycles, respectively. BOPS allows you to integrate application-specific instructions, such as multiply complex, which increases FFT performance. The five-slot VLIW engine requires many ports from the register file into each execution unit. You can configure the number of read and write ports to support your price point.

Collaboration aims for the stars

Several months ago, Lucent and Motorola announced their plans to collaborate and design a new type of DSP core. The companies crafted the basic design, the StarCore 400 architecture, using an "explicitly parallel-instruction-computing" (EPIC)

DILBERT® by Scott Adams



model. EPIC promotes the use of scalable resources, such as multiple ALUs, and a scalable instruction-set architecture. An EPIC compiler can detect parallelism and group independent instructions. Relying on the compiler to encode the parallelism minimizes the resources you need for instruction decoding and dispatch.

StarCore's basic instruction is 16 bits long, but the instruction set lets you easily build variable-length instructions by using prefixes to add capability. The use of prefixes allows StarCore to accommodate additional registers and functional units. This approach differs from VLIW, in which each instruction is a fixed length. Furthermore, the EPIC approach promotes orthogonality, unlike traditional DSPs that combine many operations in an instruction, making it difficult for a compiler to produce efficient code.

The companies based the first silicon from the StarCore program on a 0.13- $\mu$ m process and target it to operate as fast as 300 MHz. It will support four MACs per clock and integer and fractional data types. Along with software tools, the device will be available in the second half of 1999. A partnership such as this one has many obstacles to overcome, so only time will tell whether the Lucent and Motorola

project will become a rising star.

—by Markus Levy

**BOPS Inc**, Santa Clara, CA. 1-408-327-8782, www.bops.com.

Circle No. 390

**IBM Microelectronics**, Raleigh, NC. www.chips.ibm.com.

Circle No. 391

**Lucent Technologies**, Allentown,

PA. 1-800-372-2447, www.lucent.com/micro.

Circle No. 392

**Motorola**, Phoenix, AZ. 1-800-441-2447, www.mot-sps.com.

Circle No. 393

**Advanced RISC Machines**, Palo Alto, CA. 1-408-399-4826, www.arm.com.

Circle No. 394

## *Power ICs tailored to pager's demanding needs*

With their need for approximately 30-day operation from limited battery cells, pagers are among the most challenging battery-powered designs. Maxim's MAX847 and MAX769 pack many features unique to pager-system design, although you can use them for other applications, such as data loggers and transponders. Both have an SPI-compatible serial interface to control main output voltage, three low-noise regulator outputs, a three-channel A/D converter for monitoring battery levels, three DAC-controlled comparators, a low-battery detector, a beeper/vibrator driver, and a charger output for RF-power-amplifier high-current bursts.

Intended for operation from a single AA alkaline battery, the MAX847 step-up converter yields 80-mA output at 90% efficiency. In contrast, the MAX769 operates from two or three cells, functioning as a step-up/step-down converter with comparable efficiency. You can operate the devices in a fixed-frequency, 270-kHz PWM mode with low noise or synchronize their internal clocks to a frequency that is seven times an external clock's rate. The MAX847 and MAX769 ICs, both in 28-pin QSOPs, cost \$4.34 and \$5.11 (1000), respectively.

—by Bill Schweber

**Maxim Integrated Products**, Sunnyvale, CA. 1-800-998-8800, www.maxim-ic.com.

Circle No. 395

## FIBER SWITCHES AND MEDIA CONVERTERS SUPPORT ETHERNET AND FAST ETHERNET

The AT-FS20x family of two-port switches from Allied Telesyn allows you to painlessly upgrade from Ethernet to Fast Ethernet using either copper or fiber outputs. The family includes three unmanaged switches that interconnect segments of Ethernet and Fast Ethernet networks to extend and upgrade the networks and relieve network congestion. The switches integrate small workgroups with mixed 10- and 100-Mbps bandwidths. Using an external power supply, you can use an AT-FS20x as a stand-alone device; alternatively, you can install it in Allied's AT-MCR12 redundantly

powered rack-mount chassis. Unit prices for the switches range from \$249 to \$388.

A series of Allied's media converters for 100BaseTX and 100BaseFX fiber networks accommodates the MT-RJ, LC, and VF-45 next-generation, small-form-factor fiber connectors. As with the AT-FS20x family, you can use the AT-MC301/302/303 converters in stand-alone mode or in Allied's AT-MCR12 rack-mount chassis. The media converters support the MissingLink protocol, which gives the host critical information about the status of the other remote segment link. If either link fails, the converter interacts with both hosts, making each instantly aware of the link fault. Unit prices range from \$398 to \$403.—by Bill Travis

**Allied Telesyn**, Sunnyvale, CA. 1-425-481-3833, fax 1-408-736-0100, www.alliedtelesyn.com. Circle No. 396

## Hot summer delivers scorching graphics

Recent 3-D-graphics software and device announcements continue the impressive price/performance improvement trends of recent quarters. Microsoft fulfilled its promise of July availability for the final version of DirectX 6.0, including a software developer's kit. Both the software developer's kit and end-user upgrades for Windows 95 and 98 are now at [www.microsoft.com/directx](http://www.microsoft.com/directx).

Expect a slew of press releases from graphics-board and -chip manufacturers touting their higher DirectX 6-derived game-frame-rate and WinBench numbers; these numbers aren't necessarily the result of silicon or driver advancements but of Microsoft's rewritten and significantly faster software-rendering algorithms, including support for AMD ([www.amd.com](http://www.amd.com)), Cyrix ([www.cyrix.com](http://www.cyrix.com)), and Integrated Device Technology's ([www.idt.com](http://www.idt.com)), 3DNow! and Intel's ([www.intel.com](http://www.intel.com)) upcoming Katmai new instruction floating-point sets. Also, make sure that the graphics vendors, in comparing themselves with their competition are comparing apples to apples—same CPU, same graphics bus, same frame-buffer size, and same DirectX version.

3Dfx Interactive is shipping its long-rumored single-chip Voodoo Banshee 2- and 3-D graphics accelerator. Software-compatible with the company's Graphics, Rush, Voodoo and Voodoo 2 3-D-only chips which run under the Glide, DirectX and OpenGL application-programming interfaces, Banshee boasts a 100-MHz operating frequency compared with Voodoo 2's 90 MHz. However, Banshee does not support Voodoo 2's dual-chip scan-line interleaving mode and contains only one texture engine compared with Voodoo 2's two; 3Dfx devoted the silicon area instead to 2-D graphics and digital-video functions. This omission means that games that can use single-pass multitexturing when avail-

able run slower on Banshee, although the higher clock rate should improve its WinBench scores.

All Banshee graphics subsystems are 128 bits, as is the 100-MHz external-memory interface to 4- to 16-Mbyte SDRAM or synchronous graphics RAM. 3Dfx's focus on boosting 2-D graphics speed is somewhat unexpected, given the company's long-standing 3-D reputation, but it should produce noticeable performance improvements for DOS games, the Windows graphical user interface, and standard 2-D applications. The company is shipping the first-generation, \$38 (10,000) Ban-

shee with a 230- or 250-MHz RAM-DAC and a 1× Advanced Graphics Port (AGP) sideband interface. The company schedules a second-generation spin of the device to be available for sampling by year's end; that version will move to 2× AGP and a 125-MHz operating frequency. Another planned enhancement is color precision greater than 16 bits as stored in the frame buffer, which will improve visual quality, especially important when the single texture engine repeatedly reads, updates, and writes a pixel's value before displaying it to the screen.

—by Brian Dipert  
**3Dfx Interactive**, San Jose, CA. 1-408-935-4400, fax 1-408-262-8874, [www.3dfx.com](http://www.3dfx.com). Circle No. 397

### *GUI software suite simplifies embedded graphics*

Reduced hardware costs and more powerful processors are leading embedded designers away from mechanical pushbuttons and alphanumeric displays toward fully programmable graphical user interfaces (GUIs). The current trend is to put GUIs into smaller embedded systems; however, this trend has also created a software-development bottleneck. The design and implementation of an attractive GUI with an intuitive touch and feel can devour many man-hours of software support. Wind River promises to ease the development of custom GUIs with the release of two new hypertext-markup-language (HTML) graphics-development products.

One product, eNavigator, is a full Web browser targeting information-retrieval appliances, such as kiosks, televisions, set-top-boxes, and handheld devices. Wind River based eNavigator on Netscape ([www.netscape.com](http://www.netscape.com)) technology. It includes a user

interface, an HTML parsing/layout engine, support for JavaScript, and e-mail. Users can customize eNavigator to create a company-unique user interface.

The other product, HTMLworks, is a set of HTML and JavaScript components for applications running the VxWorks real-time operating system. HTMLworks includes a reference interface that developers modify to implement complex interactive GUIs for network-connected embedded devices that require no general Web-browsing function. Netscape's LiveConnect technology provides the link between the user interface and the underlying application code without interfering with the real-time operation of the device. Both eNavigator (\$10,000) and HTMLworks (\$8000) will be available this quarter.—by Warren Webb

**Wind River Systems**, Alameda, CA. 1-510-748-4100, fax 1-510-749-2010, [www.wrs.com](http://www.wrs.com).

Circle No. 398

## Configurable processor yields desktop ASIC development

Creating a custom design from off-the-shelf components is sometimes more of a challenge than your project budget can tolerate. Stringing together a  $\mu$ P, memory, and custom set of peripherals for a new embedded product usually means long

### INSTANTLY CREATE A CUSTOM DEVICE BY DRAGGING AND DROPPING SOFT IP PERIPHERALS FROM AN ONLINE LIBRARY INTO PROGRAMMABLE LOGIC.

hours in the lab and a couple of pc-board iterations before you have a working prototype.

Triscend's TE520 configurable processor promises to speed this process by allowing you to create a custom ASIC right on your desktop. The single-chip TE520 combines a microcontroller core, system RAM, a system bus, and user-programmable logic. You can customize a device to meet your embedded-system specifications.

With Triscend's FastChip processor-development software, you can instantly create a custom device by dragging and dropping soft intellectual-property (IP) peripherals from an online library into the TE520's programmable logic. Triscend's programmable logic uses SRAM-based configurable-system-logic (CSL) cells to implement the functions defined by the soft IP peripherals or user-custom logic. When the processor configuration is complete, the designer uses conventional third-party software-development tools to develop the application-program code.

The FastChip online library includes timer/counters, program-

mable I/O, UARTs, PWMs, and FIFO buffers. Users and third-party developers can create additional soft peripherals for the library by using standard EDA tools.

The TE520 contains a performance-enhanced, 40-MHz 8032 microcontroller core; 64 kbytes of on-chip system RAM, 3200 CSL cells (equal to approximately 40,000 logic gates), a 40-Mbyte/sec internal bus, and 251 user I/O pins. A single external memory holds the 8032

processor code and the CSL-configuration data.

Samples of the \$55 (100) TE520 will be available this quarter, and the company plans volume quantities for March 1999. Price of the FastChip processor-development software starts at \$495.

—by Warren Webb

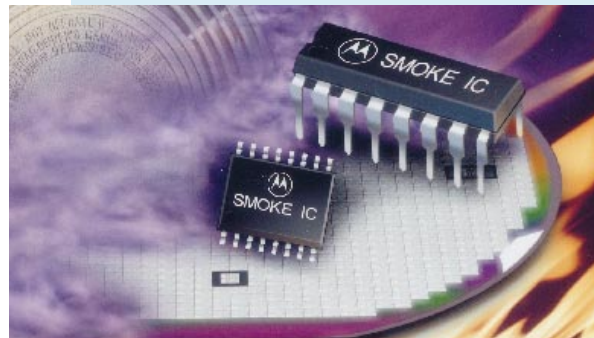
**Triscend Corp.**, Mountain View, CA. 1-650-968-8668, fax 1-650-934-9393, [www.triscend.com](http://www.triscend.com).

Circle No. 399

## IC shows where there's smoke, there's a smoke detector

Residential smoke detectors have become low cost, reliable, and commonplace in homes and offices, thanks to advances in requisite circuitry. Motorola's MC145017 "Smoke" IC provides the interface to an ionization-type smoke-detection chamber, the user-indication LED, and signal-detection/decision circuitry. Equally useful, it drives a piezoelectric horn with the distinctive 0.5-sec-on, 0.5-sec-off audio pattern that is the universal evacuation signal, meeting relevant National Fire Protection Agency, Underwriters Laboratory, and International Standards Organization standards.

Guard outputs on both sides of the detector input, an FET-input



comparator, and protection diodes provide a high-performance transducer interface. The nominal 9V IC tests its battery—a critical function for this type of alarm—not by static measurement of its battery voltage, but under dynamic load by hitting the LED with a 10-mA, 11.6-msec pulse. The \$1.50 (OEM) IC needs just a few external resistors to function, besides the ionization chamber, LED, and horn. In addition to this stand-alone IC, the otherwise-similar MC145018 allows you to interconnect as many as 40 devices and their associated detectors to a common signaling line for broad-area monitoring.—by Bill Schweber

**Motorola Semiconductor Products Sector**, Phoenix, AZ. 1-800-521-6274, <http://motorola.com/sps/>.

Circle No. 400

## Video decoding goes beyond PCs

Many industry pundits believe that except for in niche applications, the burden of digital-versatile-disk (DVD) video decoding in PCs is quickly moving from specialized logic to host-CPU-based software. Demos from all of the x86 vendors make a strong case that, at roughly 300 MHz and greater, plenty of CPU horsepower exists to smoothly display a full-frame MPEG data stream, especially if the system's graphics chip contains motion-compensation circuitry. So why did ATI Technologies put a complete video-decoding block, including not only motion compensation, but also the inverse discrete cosine transform (DCT), on its mainstream-PC-market-targeted Rage 128 architecture? It appears that the answer is that ATI's plans extend beyond the PC.

The Rage 128 product family comprises the 128 GL and 128 VR chips. They share a number of features, including a 128-bit, 2-D engine; dual 3-D engines that enable simultaneous rendering of two pixels or application of two textures to a pixel; 32-bit Z-buffer support; local memory as large as 32 Mbytes; a 230- or 250-

MHz integrated RAMDAC; 8-kbyte on-chip caches for textures *and* pixels; and a 2× sideband Advanced Graphics Port interface. The two parts differ, however, in their local-memory interfaces: The \$40 (10,000) 128 GL offers a 128-bit, 125-MHz bus to SDRAM or synchronous graphics RAM (SGRAM) in a 312-pin BGA package, whereas the \$30 (10,000) 128 VR provides a 64-bit bus in a 256-pin BGA package but interfaces with both 143-MHz standard and 250-MHz double-data-rate SGRAM.

So what about that hardware DVD decoder? ATI claims that it's useful when a high-end application, such as an elaborate computer game, might simultaneously be displaying a video stream and a 2- or 3-D user interface. Because such software is today relatively uncommon, however, and, because the inverse-DCT block probably took up a noticeable proportion of the chip's 8 million transistors, you'll probably soon see slimmed-down versions of the Rage 128 architecture. This type of integration *is* valuable, however, in digital set-top boxes which, because of their lower costs and comparatively

constrained applications, don't want or need a high-powered, flexible host CPU. Also, with 3-D-interface enhancements on the way courtesy of Microsoft's ([www.microsoft.com](http://www.microsoft.com)) ChromEffects and GDI 2000, ATI's DVD decoder may be the first example of what will become a common graphics-chip feature.

ATI offers Set-Top-Wonder-CE, a digital set-top-box reference design based on Microsoft's Windows CE operating system and ATI's 64-bit architecture. Upcoming digital set-top boxes from General Instrument ([www.gi.com](http://www.gi.com)) will also feature ATI's 128-bit graphics core. The 128 VR and 128 GL are both available for sampling and will enter full production by November. ATI will also offer three graphics boards based on the chips: the \$199, 16-Mbyte Xpert 128 and the \$299, 32-Mbyte Rage Fury and Rage Magnum. ATI plans application-programming-interface support for both DirectX 5.0/6.0 and OpenGL.—by Brian Dipert

**ATI Technologies Inc**, Thornhill, ON, Canada. 1-905-882-2600, fax 1-905-882-2620, [www.atitech.com](http://www.atitech.com).

Circle No. 401

## Monolithic instrumentation amp provides bridge from transducer's bridge

When you're dealing with noisy environments and bridge-based transducers, you likely want to use an instrumentation amplifier—normally configured from three discrete or integrated op amps—to make the transition from that differential world to conventional single-ended electronics. The AD627 instrumentation amp from Analog Devices is a micropower, single-supply, rail-to-rail device that uses an internal two-op-amp configuration to provide the function and performance of a triple-op-amp design, thus reducing cost.

Gain of this instrumentation amp is preset at

×5, but you can also set it as high as ×1000 with a single resistor. Gain accuracy is 0.10% at G+5, and drift at this gain is 10 ppm. Maximum input offset voltage is 250 μV, and maximum drift is 3 μV/°C. At 60 Hz, with 1-kΩ source imbalance, CMRR is at least 83 dB. You can power this eight-pin IC from a single 3 to ±15V supply; maximum supply current is 85 μA. The AD627 costs \$2.20 (1000).

—by Bill Schweber

**Analog Devices Inc**, Norwood, MA. 1-781-937-1428, fax 1-781-821-4273, [www.analog.com](http://www.analog.com).

Circle No. 402

## Count on Talisman for graphics good luck

Microsoft ([www.microsoft.com](http://www.microsoft.com)), along with several partners, launched its Talisman graphics initiative with great fanfare at the 1996 Siggraph show. The initiative's name is ironic, however, since the project has been plagued with plenty of bad karma over the last two years. Reference-design schedules have slipped and faced cancellation, and silicon vendors have defected. Coincident with this rough start-up, conventional graphics engines have achieved tremendous performance gains and cost reductions; CPU-to-graphics chip bandwidth has exploded, thanks to the Advanced Graphics Port (AGP); and graphics memory is faster and cheaper than ever. Is there still room in the graphics market for a nonstandard approach?

Fujitsu apparently thinks so, and the company will soon make its first Talisman-based graphics chip, the Marquis 2000, available for sampling and slates full production for mid-1999. Marquis 2000 varies from Microsoft's original vision in a few areas; it has no separate media processor or 1394 interface, for example. However, the company has made one key enhancement that will increase its potential for success: a baseline "virtual-frame-buffer" compatibility mode that lets the device run DirectX and OpenGL applications without alteration.

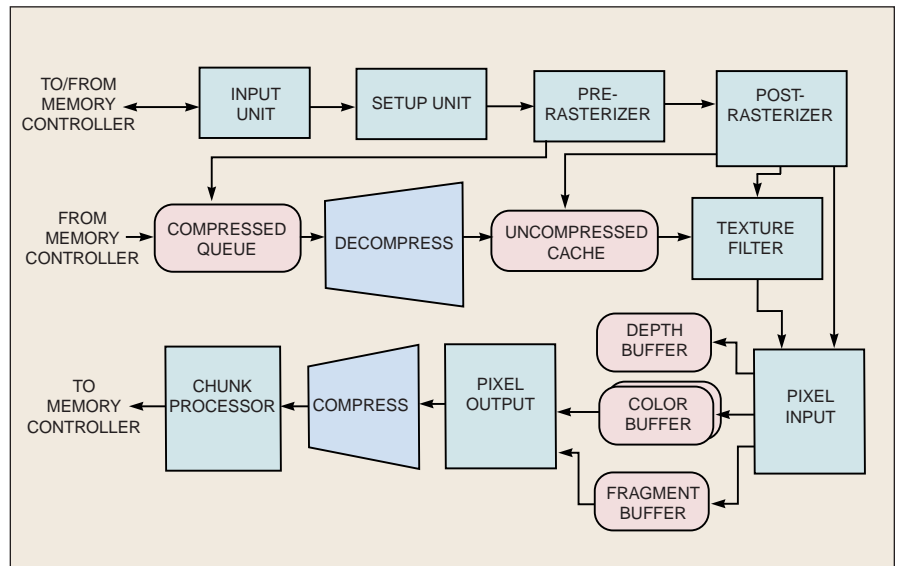
Anticipated compatibility-mode specifications are nothing to scoff at. They include a 2x AGP sideband interface; full digital-versatile-disk (DVD) decoding (which Fujitsu may omit in future versions to cut costs in this era of software-based DVD); and an integrated RAMDAC that provides 1600x1200-pixel, true-color resolution at 85 Hz. Fujitsu predicts a 125 million- to 140 million-pixel/sec, single-pipeline, 2-D and 3-D, 32-bit color-fill rate with trilinear MIP mapping, full-scene antialiasing, and other high-quality image features enabled, or roughly

twice that fill rate using bilinear filtering. However, enhanced application-programming interfaces that can take full advantage of the Fujitsu chip's capabilities may see even higher performance and image quality.

Marquis 2000 breaks the frame to be displayed into 32x32-pixel chunks not unlike the tile-based rendering scheme of NEC's ([www.nec.com](http://www.nec.com)) PowerVR architecture or the even finer grained Stellar Semiconductor ([www.stellarsemi.com](http://www.stellarsemi.com)) Pixel-Squirt approach. The chip applies *all* decompressed anisotropic-filtered tex-

ing scene objects as separate entities, called "layers," or "sprites," and updates the display only for those objects that change from one frame to the next instead of rerendering the entire screen. For multichunk bit maps that change only slightly (in position or orientation), Marquis 2000 applies an affine map transform instead of using the time-consuming full 3-D rendering pipeline.

Fujitsu estimates that the scene-dependent performance resulting from Talisman enhancements could be as much as three to five times better than that of compatibility



The Talisman architecture implements a radically different form of the 2-D/3-D rendering pipeline from that of traditional graphics devices.

tures and other color, alpha, depth, and antialiasing effects before compressing and writing the pixel array to local memory, or the "compositing buffer." By not repeatedly reading, altering, and rewriting pixel information to the frame buffer before displaying it, Fujitsu's approach claims to improve image quality (by minimizing rounding errors) and to more efficiently use available system bandwidth and memory density.

Marquis 2000 treats nonintersect-

mode. The company targets less than \$40 (10,000) for production silicon. This price could go lower if the production stepping also involves shrinking the lithography. DirectX and OpenGL drivers are under development, and Fujitsu anticipates that Microsoft will rapidly add Talisman enhancements to a DirectX 6 upgrade version.—by Brian Dipert

**Fujitsu Microelectronics**, San Jose, CA. 1-408-922-9000, fax 1-408-943-0403, [www.fujitsu.com](http://www.fujitsu.com).

Circle No. 403

## Reconfigurable computing speeds chip-design verification

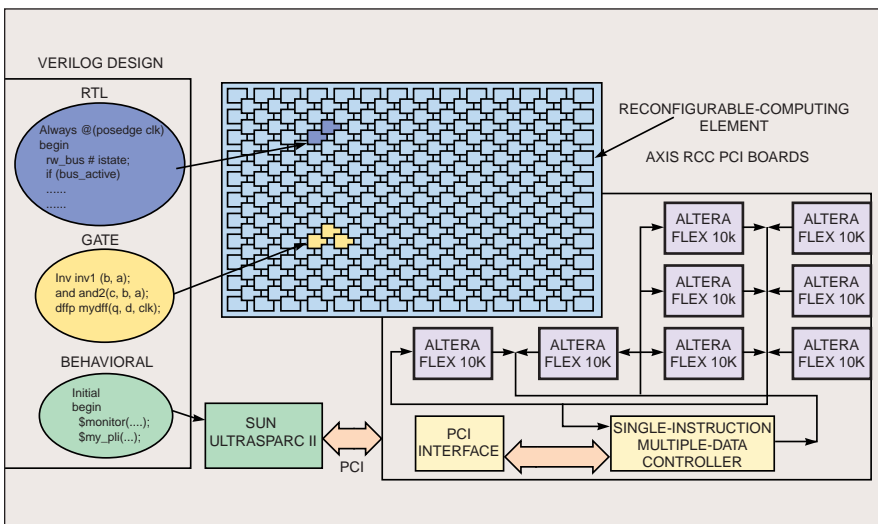
Axis Systems has entered the chip multilevel-verification market with its Xcite-1000 system. By using reconfigurable-computing (RCC) technology, Xcite-1000 maps your Verilog design at RTL and behavioral and gate levels into programmable-logic-based chips. When you simulate the mapped design, it looks and acts as if it were running on a software simulator but has the speed advantage of hardware-based simulation.

After partitioning and compiling your multilevel HDL design, Xcite-1000 reconfigures programmable-logic chips as design-specific computing blocks for the gate-level and RTL portions of your design. The hardware-based simulation runs at 10,000 to 100,000 cycles/sec—much faster than gate-level or RTL software-based simulations. A software simulator running on the host computer simulates the behavioral portion of your design. If you find a problem during gate-level or RTL simulation, you can quickly and easily swap simulation states between the RCC hardware and a software simulator and then use software simulation to help debug the design.

Xcite-1000 RCC is similar to that of Quickturn's ([www.quickturn.com](http://www.quickturn.com)) Mercury, a self-contained system containing FPGA-based reconfigurable computing along with other hardware and software to boost simulation speed. Unlike Mercury, Xcite-1000 hardware resides on pc boards that mount in Sun workstations. Each board handles designs having as many as 250,000 gates using Altera ([www.altera.com](http://www.altera.com)) 10K250 programmable-logic chips. It also includes 8 Mbits of memory on each board to simulate memory models. Each workstation handles as many as eight Xcite-1000 boards.

Xcite-1000 runs on Sun Microsystems Ultrasparc30 and Ultrasparc60 workstations. A 1 million-gate system with software simulator and RCC compiler costs \$295,000. You can get systems with capacities as high as 2 million gates for \$390,000, and Axis will offer a 4 million-gate system by December. Axis is developing a VHDL version of Xcite.—by Jim Lipman

**Axis Systems**, Sunnyvale, CA. 1-408-588-2000, fax 1-408-588-1662, [www.axiscorp.com](http://www.axiscorp.com). Circle No. 404



The Xcite-1000 partitions your design into various levels of design abstraction. The system maps gate-level and RTL portions of the design into Altera chips, which are reconfigured as design-specific computing elements. The hardware-based simulations run much faster than software-based gate-level or RTL simulations.

## LVDS enclosure family supports Ultra2 bus speeds

The Ultra2 3000 Series of low-voltage-differential storage enclosures from Trimm Technologies supports 10,000-rpm, single-connector-attachment (SCA) drives at Ultra2 bus speeds. The enclosure uses low-voltage differential signaling (LVDS), providing 80-Mbyte/sec data-transfer rates and accommodating cable as long as 12m. You can easily mount standard, 1.65-in. or low-profile, 1-in. drives into the enclosures' hot-swap, field-replaceable drive trays. The same drive canisters appear in all four models of the family, which includes two- and four-high tabletop and eight-high tower and eight-drive rack-mount configurations. In the tower and rack-mount models, you can choose the standard configurations of two or four drives per bus with preset address and bus termination. In addition, a supplied jumper cable lets you quickly convert the enclosure to a single eight-drive bus with address switches and HD68 connectors on the rear of the chassis. Unit prices start at \$667 for the two-bay model.

—by Bill Travis  
**Trimm Technologies**, Las Vegas, NV. 1-702-263-2310, fax 1-702-361-6067, [www.trimm.com](http://www.trimm.com). Circle No. 405



Low-voltage differential signaling allows 80-Mbyte/sec data rates in Trimm's storage enclosures.

## Single-supply line driver makes ADSL G.lite bits swim upstream

Asymmetrical-digital-subscriber-line (ADSL) technology requires high-power DSP computation, but it also needs significant analog current sourcing and sinking when the signal meets the line. Using the 5V-only DRV1101 line driver from Burr-Brown, you can simplify building the upstream ADSL G.lite circuitry that drives the line-interface transformer to push signals from the end user to the central office (see "ADSL chip sets trim down with G.lite," *EDN*, July 2, 1998, pg 81).

The 10-MHz, eight-pin SOIC supplies as much as 230 mA of peak output current with an output voltage swing of 7V p-p. In a typical installation, the fixed-differential-gain (3V/V) IC supplies 10-dBm average line power with a crest factor of 5.3, corresponding to a peak delivered line power of roughly 25 dBm. ADSL also demands low distortion: THD for this device is -81 dBc with a 100 kHz, 6V p-p output into 100Ω. The DRV1101 costs \$2.95 (1000).—by Bill Schweber

**Burr-Brown Corp.**, Tucson, AZ. 1-520-746-1111, fax 1-520-746-7401, [www.burr-brown.com](http://www.burr-brown.com). Circle No. 406



Optimized for driving ADSL G.lite signals upstream, the Burr-Brown DRV1101 line driver can push as much as 230 mA of peak current at wideband and low distortion.

## Keep your technical skills sharp with free, Web-based school

Using the resources of the TechOnLine University (TOLU), you can take free technology courses in 30-minute interactive modules based on a customized, personal learning plan. Instructors, including university professors and industry experts, cover topics such as xDSL, wireless links, DSP and DSP tools, and communications standards; every month, TechOnLine adds other courses focusing on theory, applications, products, and technologies.

Vendors and ads sponsor the courses, which are not necessarily tied to specific products; in fact, some of the topics, such as those discussing technical standards, are not closely associated with any vendor. However, some sponsors show how you can use their products to implement application examples. Each module includes interactive exercises and a closing self-test that helps you decide whether you should move to the next module.

—by Bill Schweber

**TechOnLine Inc.**, Waltham, MA. 1-781-642-1600, [www.techonline.com](http://www.techonline.com).

Circle No. 407

## Calendar

Oct 29 to 30

**Communication Design Engineering Conference**, San Jose, CA, focuses on network-hardware implementations from ASICs to finished systems. The conference offers 24 technical classes addressing practical techniques and methods for developing hardware and software for network-communication applications. One- and two-hour classes cover asynchronous digital-subscriber line, voice over the Internet, asynchronous-transfer-mode, and modulation techniques. Registration costs \$795. Miller Freeman Inc, San Francisco, CA. 1-415-538-3848.

Nov 1 to 5

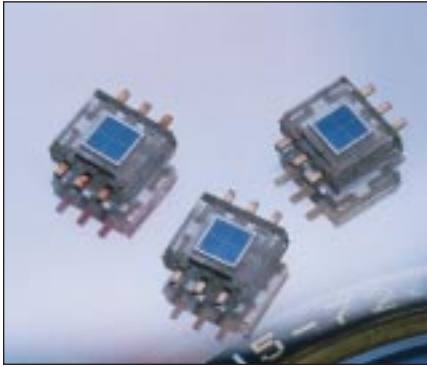
**Embedded Systems Conference**, San Jose, CA, offers 148 classes and 12 full-day tutorials. Topics include DSP and wireless technologies, C and C++ real-time programming, debugging strategies, kernels, interrupt handling, Web-based management of networked devices, and Windows CE. New offerings include intelligent distributed control, Firewire, and virtual memory. More than 280 vendors exhibit embedded-system products and services. Registration for the five-day tutorials-and-conference program costs \$1645. Miller Freeman Inc, San Francisco, CA. 1-415-538-3848.

Nov 2 to 4

**Power Electronics: Circuits and Systems**, Madison, WI, lets you compare converter types, apply power-semiconductor devices, protect semiconductor components in power-electronic circuits, analyze power-electronic systems with various types of load, explore modulation strategies, study interaction modes, and study trends. Department of Engineering Professional Development, University of Wisconsin—Madison. 1-800-462-0876.

## PIN photodiode positions CDs in optical drives

The S6695 silicon-quadrant (quadruple) PIN photodiode from Hamamatsu provides the photosensitivity and spectral response suitable for positioning and stabilizing CDs in optical disk drives. The surface-mount device measures 4.8×1.8×4.1 mm and operates over -25 to +85°C. Its spectral response covers 320 to 1060 nm with peak sensitivity at 900 nm. Photosensitivity is 480 mA/W at 680 nm and 550 mA/W at 780 nm. Dark current is typically 0.1 nA, and terminal capacitance is typically 4 pF with 5V reverse voltage applied. The S6695 costs less than \$2 (OEM).—by Bill Travis



A quadrant photodiode from Hamamatsu uses red-LED triangulation to position and stabilize CDs in optical drives.

Hamamatsu Corp, Bridgewater, NJ. 1-908-231-0960, fax 1-908-231-1218. Circle No. 408

## Low FET resistance and gate charge boost efficiency in switchers

A family of HexFET power MOSFETs from International Rectifier lays claim to the industry's lowest on-resistance and gate charge. The 500 to 650V devices, intended for offline switching power supplies, claim on-resistance ratings as much as 50% lower and gate charge approximately 33% lower than previous FETs. They can thus reduce switching, conduction, and drive losses by as much as 30% in a power supply, thereby allowing you to use smaller heat sinks or coolers within a thermal system. The MOSFETs have topology-specific data sheets that provide ratings of interest to switching-power-supply designers. Prices start at 60 cents (100,000).—by Bill Travis

International Rectifier, El Segundo, CA. 1-310-252-7105, fax 1-310-252-7903, www.irf.com. Circle No. 409

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## RATE ADAPTERS BRIDGE EMULATION PROBLEMS

The application-specific SpeedBridge rate-adaptor family from Quickturn combine hardware and software to provide a controlled data transfer between the company's emulation systems and your target system. Each box allows you to run the target system, often a PC, at normal or near-normal speeds, simplifying system control and debugging.

The Ethernet adapter, a PCI-based network-interface card, supports bidirectional, full-duplex 10/100-Mbit Ethernet with an interface speed of 100 kHz to 25 MHz. PCI SpeedBridge connects emulated PCI designs to standard PCs through a PCI bus and supports 33-

MHz PCI, Revision 2.1. The Advanced Graphics Port (AGP) adapter connects emulated AGP designs to standard PCs through an AGP bus. RGB SpeedBridge includes a video-frame buffer, connects emulation-speed video data to monitor-ready analog or digital data streams, and supports screen resolutions as high as 1920×1200 pixels. SpeedBridge prices are \$15,000 for Ethernet, \$50,000 for PCI, \$50,000 for Advanced Graphics Port, and \$20,000 for RGB.—by Jim Lipman

Quickturn Design Systems, San Jose CA. 1-408-914-6000, fax 1-408-914-6001, www.quickturn.com.

Circle No. 410