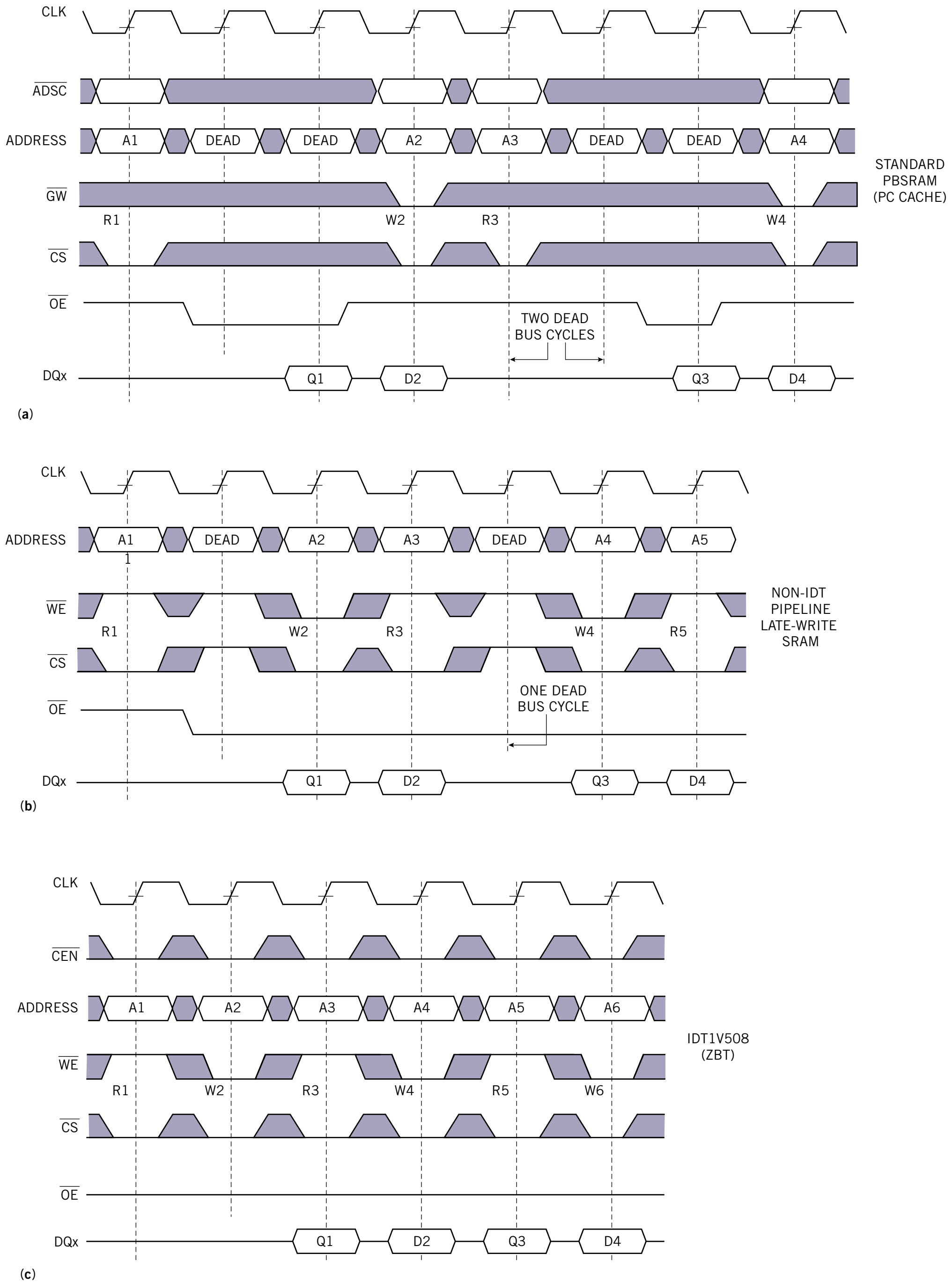


Figure 2



Standard (a), late-write (b), and no-latency (c) synchronous SRAMs make incremental improvements in sustained data-bus bandwidth when the system switches between write and read operations (courtesy Integrated Device Technology).