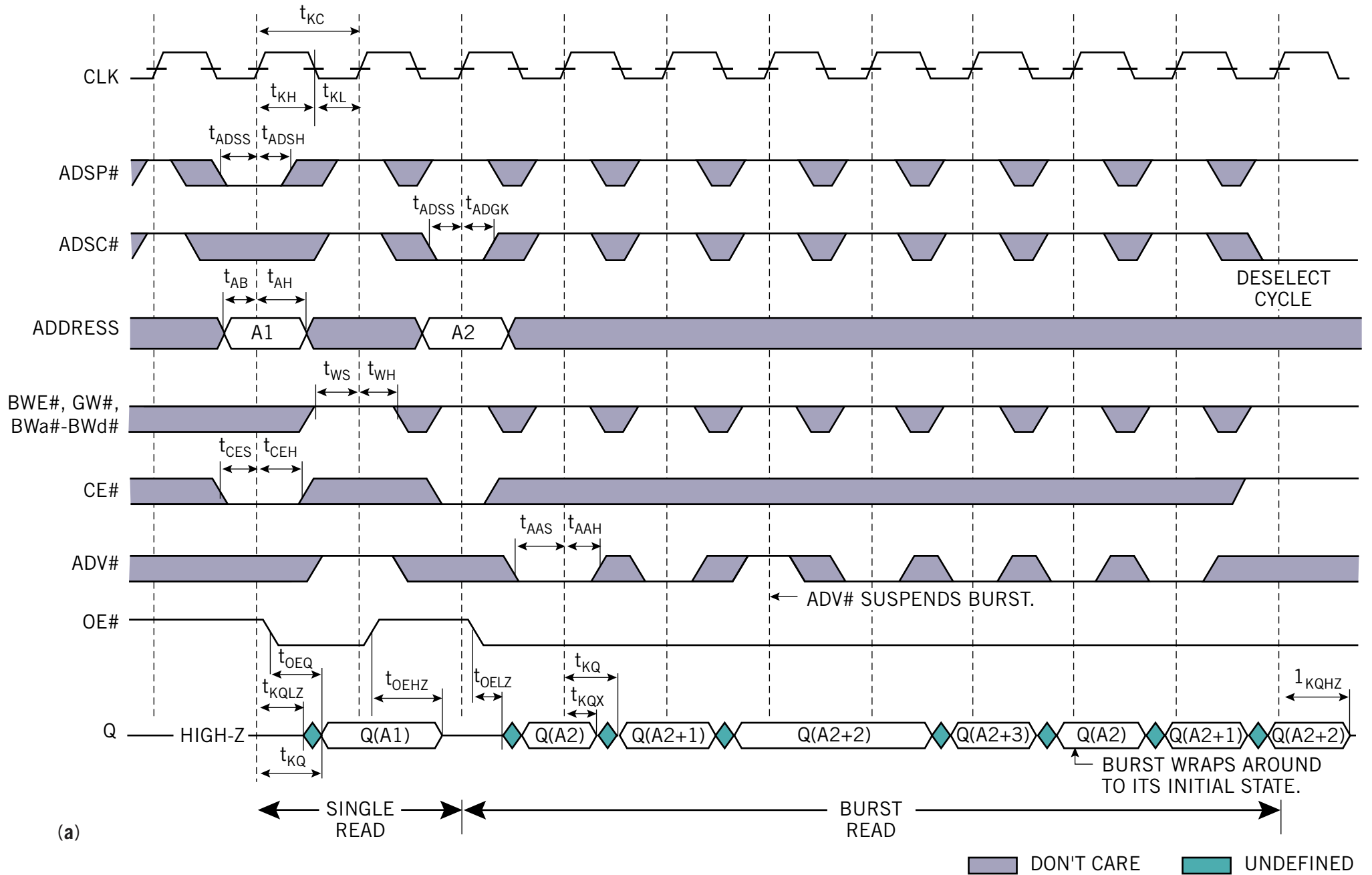
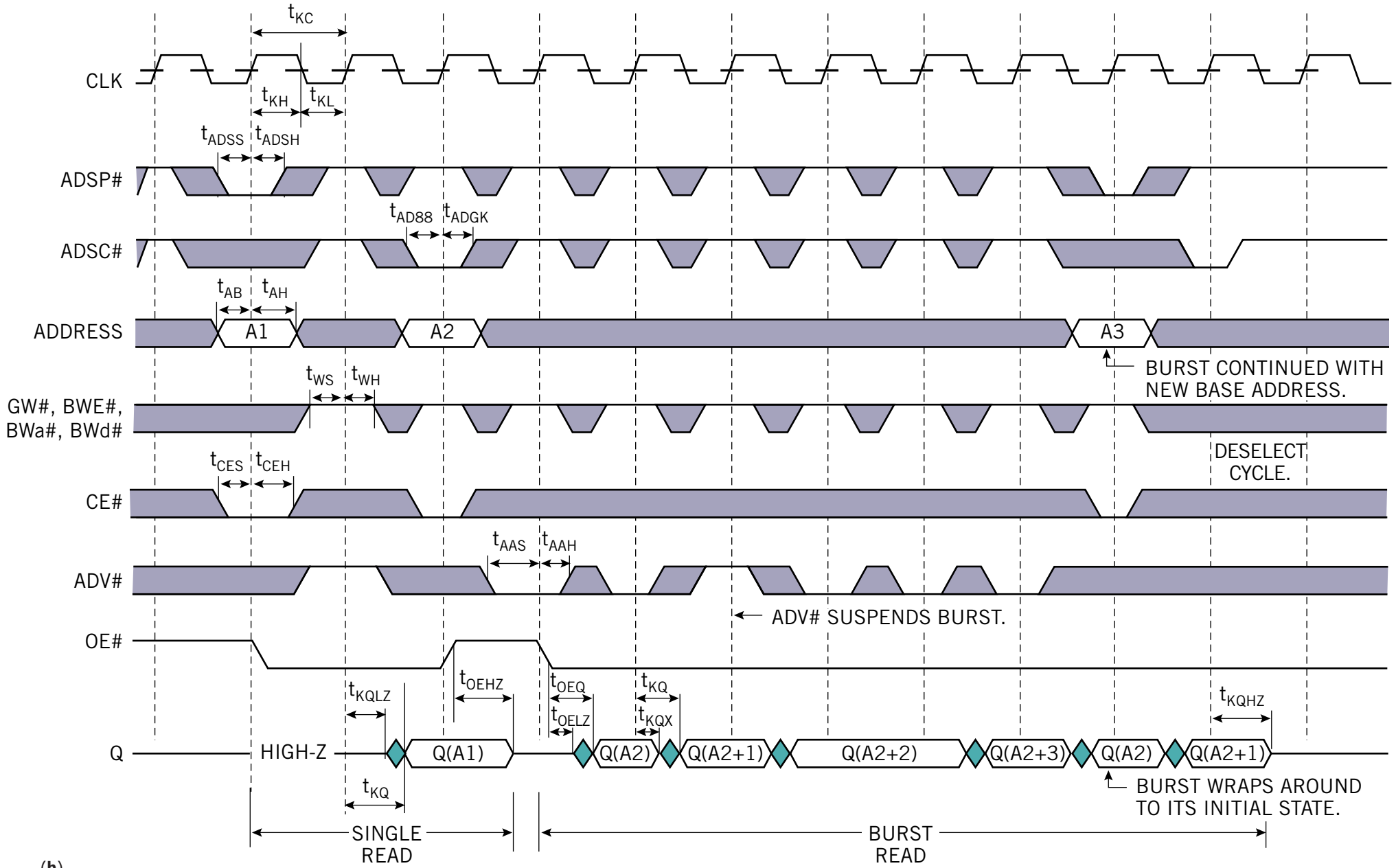


Figure 1a



Flow-through synchronous SRAMs in (a) (bottom of pg 64) enable fast bus turnaround between reads and writes, whereas pipelined alternatives (b) exhibit an additional one-clock read-access latency because of their on-chip register bank (c) but frequently run at higher clock frequencies (a and b courtesy G-Link Technology).

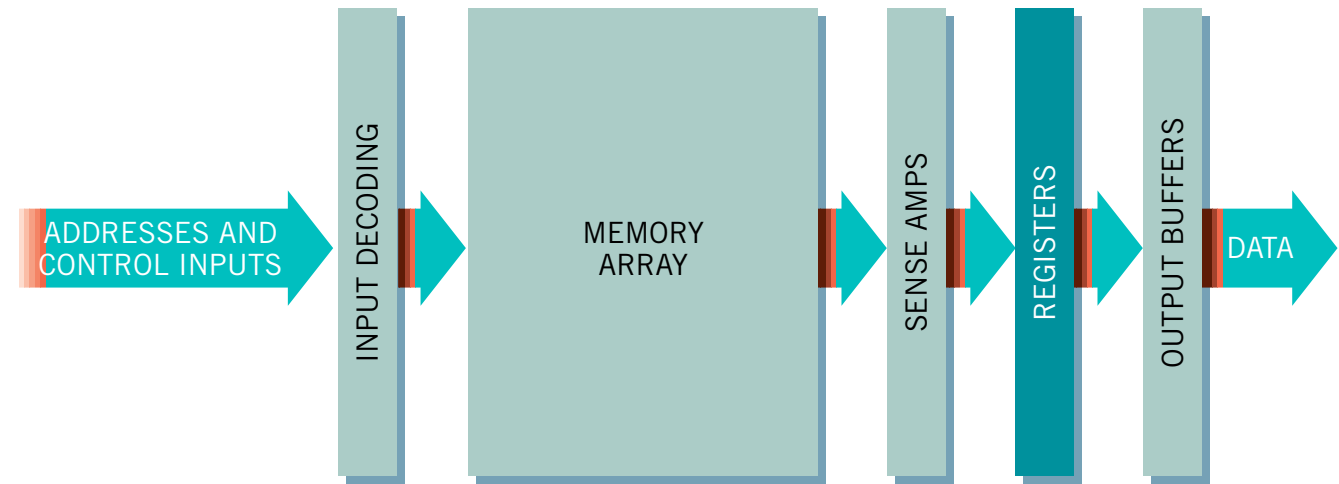
Figure 1b



(b)

Flow-through synchronous SRAMs in (a) (bottom of pg 64) enable fast bus turnaround between reads and writes, whereas pipelined alternatives (b) exhibit an additional one-clock read-access latency because of their on-chip register bank (c) but frequently run at higher clock frequencies (a and b courtesy G-Link Technology).

Figure 1c



(c)

**Flow-through synchronous SRAMs in (a) (bottom of pg 64) enable fast bus turnaround between reads and writes, whereas pipelined alternatives (b) exhibit an additional one-clock read-access latency because of their on-chip register bank (c) but frequently run at higher clock frequencies (a and b courtesy G-Link Technology).**