

WHEN YOU DESIGN A DIGITAL RECEIVER, YOU NEED TO LOOK AT SOME CONVENTIONAL PERFORMANCE PARAMETERS IN A NEW WAY, AND YOU NEED TO EXAMINE FACTORS THAT ARE UNIQUE TO THIS ARCHITECTURE.

Digital-radio-receiver design requires re-evaluation of parameters

The traditional radio architecture, which uses analog circuitry to tune, downconvert, and even demodulate the desired signal, has been the mainstay of communications for more than 50 years. In the past few years, though, the digital radio and digital receiver have become increasingly popular, as improved components, such as A/D converters and cost-effective and powerful DSPs, have become available. To effectively use digital circuitry in a radio and a receiver, you need to understand how current performance measures apply to this new architecture and what new measures you need for a more complete system design and a better understanding of that design.

Traditionally, a radio has been the “box” that connects to the antenna and to everything behind the antenna. However, many system designs are segmented into two subsystems: the radio and the digital processor. With this segmentation, the digital processor aims to extract the desired information from the digitized data. A digital receiver is not the same thing as a digital radio (demodulation). The purpose of a digital radio is to downconvert and filter the desired signal and then to digitize the information. In contrast, a digital receiver can also receive and recover any analog signal, such as those signals with amplitude or frequency modulation.

You need to consider the single-carrier receiver and the multicarrier types of receiver. The single-carrier re-

ceiver is a traditional radio receiver, deriving its selectivity in the analog filters of the IF stages. The multicarrier receiver processes all signals within the band with a single RF/IF analog strip and derives selectivity within the digital filters that follow the ADC. The benefit of such a receiver is that it eliminates redundant circuits in applications with multiple receivers tuned to different frequencies within the same band; therefore, it reduces both the sizes and the costs of the system designs.

RECEIVER-PERFORMANCE EXPECTATIONS

Your analysis begins with a generic receiver design that spans from an antenna at one end to the digital tuner/filter at the other end (Figure 1). First, assume that the receiver is noise-limited, with no in-band spurs that would otherwise limit performance. This assumption is reasonable, because you can choose the local oscillator and IF. Additionally, spurs that are generated within the ADC are usually not a problem, because you can eliminate them by adding dither, by carefully using oversampling, or by carefully choosing your signal placement. These assumptions may be unrealistic in some cases, but they provide you a starting point to benchmark performance limits.

Second, assume that the bandwidth of the receiver front end is the Nyquist bandwidth. Although your allocated bandwidth may be only 5 MHz, for example,

The basic radio comprises a series of stages between the antenna and the ADC, which feeds data to the DSP.

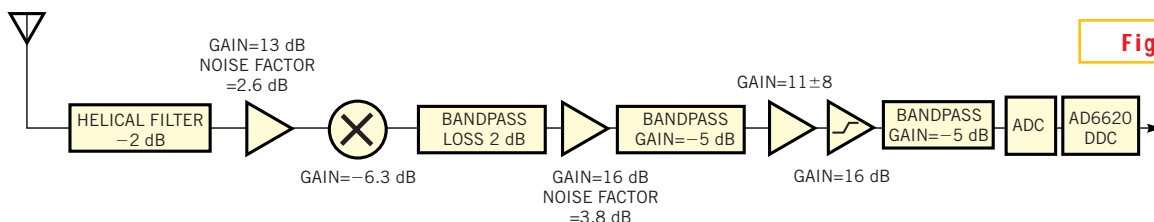


Figure 1

you can use the Nyquist bandwidth to simplify computations along the way. Using this assumption, a sample rate of 65M samples/sec gives you a Nyquist bandwidth of 32.5 MHz.

AVAILABLE NOISE POWER

To start the analysis, you must consider the noise at the antenna port. Because a properly matched antenna appears resistive to the receiver front end, use the following well-known equation to determine the noise voltage across the matched input terminals:

$$V_n^2 = 4kTRB,$$

where k is Boltzmann's constant (1.38×10^{-23} J/K), T is the temperature (in degrees Kelvin), R is the resistance (in ohms), and B is the bandwidth (in hertz). The power available from the source (in this case, the antenna is the source) is:

$$P_a = \frac{V_n^2}{4R}.$$

When you substitute the previous equation, the above equation simplifies to:

$$P_a = kTB.$$

Thus, in this case, the available noise power from the source is independent of impedance for non-zero and finite-resistance values. This calculation is important because it is the reference point with which you compare your receiver. When dealing with the noise figure of a stage, technical specifications often state that noise exhibits "x" dB above "kT" noise. The previous power equation is the source of that expression.

As it passes through each progressive stage of the receiver, the noise figure of the stage degrades the overall noise figure. When you tune and filter the channel, you remove much of the noise, leaving only the noise that

lies within the channel of interest.

The noise figure describes how much noise the receive chain of a radio adds to a signal. It is usually specified in decibels, although in the computation of the noise figure, you use the nonlogarithmic numerical ratio. The following equation defines the nonlog, or noise factor, which is usually denoted as F :

$$F = \frac{SNR_{OUT}}{SNR_{IN}}.$$

Once you assign noise figures to each of the stages in a radio, you can use the figures to determine the cascaded noise performance. You can compute the total noise factor, referenced to the input port, from:

$$F_{TOTAL} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \frac{F_4 - 1}{G_1 G_2 G_3} + K$$

The Fs are the noise factors for each of

the serial stages, and the Gs are the gains of the stages. At this point, neither the noise factors nor the gains are in log form. When you apply the above equation, it reflects all component noise to the antenna port. Thus, you can directly determine the available noise from the previous section, P_a , by using the noise figure:

$$P_{TOTAL} = P_a + NF + G.$$

For example, if the available noise (P_a) is -100 dBm, the computed noise figure (NF) is 10 dB, and conversion gain (G) is 20 dB, then the total equivalent noise at the output (P_{TOTAL}) is -70 dBm.

You should consider several points when you apply these equations. First, for passive components, you should assume that the noise figure equals the loss of the passive components. Second, you can sum passive components in series before you apply the above equation. For example, if two low-pass filters are in series, and each filter has an insertion loss of 3 dB, you can combine the filters into a single element with loss of 6 dB. Finally, manufacturers do not often assign a noise figure to their mixers. If a manufacturer does not specify a figure, you can use the insertion loss. However, if the manufacturer does supply a noise figure for its device, you should use it.

NOISE FIGURES AND A/D CONVERTERS

Although you could assign a noise figure to the ADC, it is often easier to work with the ADC in a different way. ADCs are voltage devices, whereas noise figure is really a noise-power issue. It is often easier for you to analyze the analog sections in noise figures and then convert to voltage at the ADC. Then, convert the ADC's noise into an input-referenced voltage. Finally, sum the noise from the analog signal and ADC at the ADC input to find the total effective noise.

This application uses an ADC such as the Analog Devices AD9042 or AD6640 12-bit converters with full-scale input range of 0.707V. These converters can sample at 65M samples/sec, a rate suitable for Advanced Mobile Phone Services (AMPS) digitization across the entire band, and they are also capable of 5x reference clock rate for Global System for Mobile communications

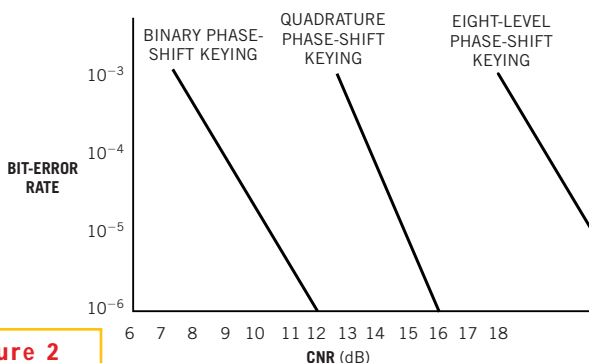


Figure 2

You can expect a bit-error rate that is a function of both the CNR and the system modulation that you use for the data.

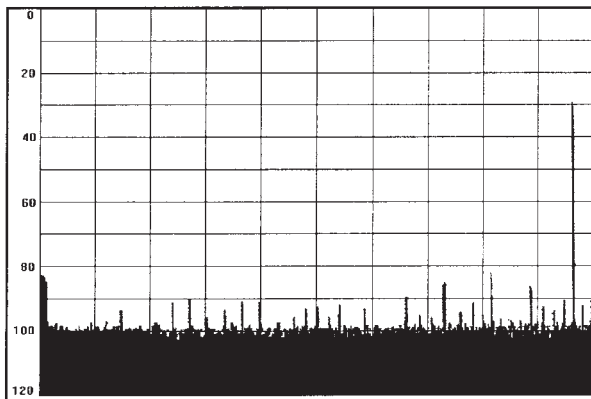


Figure 3

Before you apply dither to the input signal, the ADC performance shows a noise floor of around -100 dBc, plus some spurs throughout the spec-trum at -80 to -90 dBc.

(GSM) systems. This sampling rate is also more than adequate for AMPS, GSM and CDMA applications.

The data sheet gives the typical SNR as 68 dB. Your next step is to calculate the noise degradation within the receiver that results from ADC noise. Again, the simplest method is to convert both the SNR and the receiver noise into rms volts and then sum them for the total rms noise. For example, if an ADC has a 2V p-p input range, then

$$V_{\text{NOISE}}^2 = (0.707 \cdot 10^{-\text{SNR}/20})^2,$$

or $79.22 \times 10^{-9} \text{ V}^2$.

This voltage represents all noises, thermal and quantization, within the ADC.

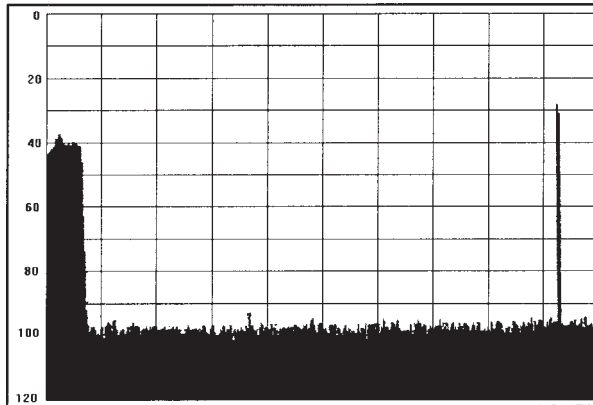
Once you compute the ADC equivalent input noise, you can compute the noise that the receiver generates. Because you assume that the receiver bandwidth is the Nyquist bandwidth, a sample rate of 65M samples/sec produces a bandwidth of 32.5 MHz. From the available noise-power equations, noise power from the analog front end is $134.55 \times 10^{-15} \text{ W}$, or -98.7 dBm . This noise is present at the antenna. You must first “gain up” the noise by the conversion gain, but the noise figure further degrades the conversion gain. If conversion gain is 25 dB and the noise figure is 5 dB, then the noise presented to the ADC input network is: $-98.7 \text{ dBm} + 25 \text{ dB} + 5 \text{ dB} = -68.7 \text{ dBm}$, or $134.9 \times 10^{-12} \text{ W}$, into 50Ω .

Because the ADC has an input impedance of about 1000Ω , you must either match the standard 50Ω IF impedance to this value or pad down the ADC impedance. To compromise, you should pad down the range to 200Ω with a parallel resistor and then use a 1-to-4 transformer to match the rest of the impedance difference. The transformer also converts the unbalanced input to the balanced signal that the ADC requires and provides some voltage gain. A 1-to-4 step-up in impedance results in a corresponding voltage gain of 2. Thus, $V^2 = \text{PR}$.

From this equation, your voltage squared into 50Ω is 6.745×10^{-9} , or 26.98×10^{-9} into 200Ω .

Now that you know the noise from the ADC and the RF front end, you can com-

Figure 4



By adding dither to the signal, you can greatly reduce the spurs that rise from the noise floor.

pute the total noise in the system by calculating the square root of the sum of the squares. Thus, the total voltage is $325.9 \mu\text{V}$. This value is the total noise present in the ADC, including receiver, ADC, and quantization noise.

CONVERSION GAIN AND SENSITIVITY

How does noise voltage contribute to the overall performance of the ADC? Assume that only one RF signal is present in the receiver bandwidth. The SNR would then be:

$$20\log(\text{SIG}/\text{NOISE}) =$$

$$20\log(0.707/325.9 \cdot 10^{-6}) = 66.7.$$

This is an oversampling application, and the actual signal bandwidth is much less than the sample rate; therefore, digital filtering greatly reduces noise. Because the front-end bandwidth is the same as ADC bandwidth, both ADC noise and RF/IF noise improve at the same rate. Many communications standards support narrow-channel bandwidths, so assume a 30-kHz channel. Therefore, you gain 30.4 dB from process gain, and the original SNR of 66.7 dB is now 97.1 dB. Remember that process gain increases SNR because the gain spreads the noise bandwidth, after which you apply a narrow-bandwidth filter.

In a multicarrier radio, the ADC must share its dynamic range with other RF carriers. For example, if eight carriers have equal power, each signal should be no more than one-eighth of the total range, or -18 dBc , if you consider peak-to-peak signals. However, because the signals are normally not in phase with one another among re-

ceivers (because handsets are not phase-locked), the signals rarely if ever align. Therefore, a peak that is less than -18 dB of the total range satisfies your requirements.

In addition, only two signals normally align at once, and, because these are modulated signals, you need reserve only 3 dB (5 to 6 dB for a conservative design) for head room. In the event that signals do align and cause the converter to clip, the clipping occurs for only a fraction of a second before the circuitry clears the overdrive condition. A single carrier radio requires no head room.

Depending on the modulation scheme, the radio requires a minimum carrier-to-noise ratio (CNR) for adequate demodulation. If the modulation scheme is digital, you must consider the bit-error rate (Figure 2). If you assume that the radio requires a minimum CNR of 10 dB, your input-signal level cannot be so small that the remaining SNR is less than 10 dB. Thus, the signal level may fall 87.1 dB from its current level. The ADC has a full-scale range of 4 dBm (200Ω); therefore, the signal level at the ADC input is -83.1 dBm . If 25 dB of gain were in the RF/IF path, receiver sensitivity at the antenna would be $-83.1 \text{ dBm} - 25 \text{ dB}$, or -108.1 dBm . If your design requires more sensitivity, you can increase gain in the RF/IF stages. However, noise figure depends on gain, and an increase in gain may adversely affect noise performance from additional gain stages.

ADC SPURIOUS SIGNALS AND DITHER

A noise-limited example does not adequately demonstrate the true limitations of a receiver. Other limitations, such as spurious-free dynamic range (SFDR), are more restrictive than SNR and noise. Assume that the ADC has an SFDR specification of -80 dB full scale, or -76 dBm (because full scale is 4 dBm). Also, assume that a tolerable carrier-to-interferer ratio (CIR) is 18 dB. (Note that CIR differs from CNR.) Based on this assumption, the minimum signal level is -62 dB full scale ($-80+18$) or -58 dBm . At the antenna, the signal level is -83 dBm ($-58-25$). Therefore, single or multitone SFDR would limit receiver performance long before noise limits it.

Adding dither can greatly improve SFDR. The addition of out-of-band noise can improve SFDR well into the noise floor (Reference 1). Although the amount of dither is converter-specific, the technique applies to all ADCs in which static differential nonlinearity limits performance, rather than ADC problems, such as slew-rate limiting. In the AD9042 ADC, the amount of added noise is only -32.5 dBm, or 21 converter codes (rms).

The “before” and “after” dither plots provide insight into the potential for improvement (figures 3 and 4). In simple terms, dither works by randomizing the coherent spurious signals that are generated within the ADC. You must conserve the energy of the spurs; dither simply causes the spurs to appear as additional noise in the floor of the converter. This additional noise appears in the before and after dither plots as a slight increase in the average noise floor of the converter. The trade-off you make by using out-of-band dither is that you can remove literally all internally generated spurious signals, but there is a slight degradation in the overall SNR of the converter. In practical terms, this degradation amounts to much less than 1 dB of sensitivity loss, which is less than the noise-limited example and is much better than the SFDR-limited example.

You need to remember two important points about dither. First, in a multicarrier receiver, you can expect that none of the channels are correlated. If this expectation is true, the multiple signals serve as a self-dither source for the receiver channel. If this expectation is false, you need to add dither when signal strengths are weak. Second, the noise contributed from the analog front end alone is insufficient to dither the ADC. In the example above, adding -32.5 dBm of dither yields an optimum improvement in SFDR. In comparison, the analog front end provides only -68 dBm of noise power, far from what you need to achieve optimum performance.

THIRD-ORDER INTERCEPT POINT

In addition to converter SFDR, the RF section contributes to the spurious performance of the receiver. Techniques such as dither do not affect these spurs, and you must address them separately to prevent disruption of receiver performance. Third-order intercept is an important parameter because the signal levels within the receiver

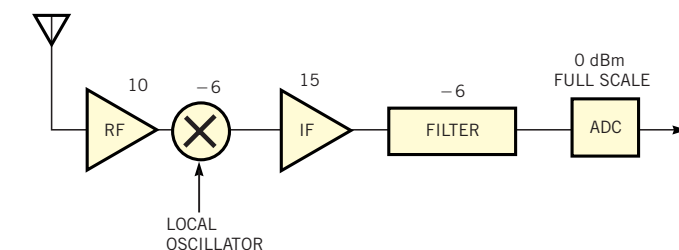


Figure 5

When analyzing third-order input intercept, you allocate gains and losses among the signal chain functional blocks.

chain increase as they pass through the receiver.

To determine what level of performance you need from wideband RF components, use the GSM specification, which is one of the most demanding receiver applications. A GSM receiver must be able to recover a signal with a power level of -13 dBm and -104 dBm. Assume that the full-scale range of the ADC is 0 dBm and that losses through the receiver filters and mixers are each 6 dB. Also, because the radio must simultaneously process multiple signals, you should not use an AGC. Using an AGC would reduce RF sensitivity and cause the radio to drop the weaker signal. Working with this information, you calculate that the RF/IF gain needed is 25 dB by: Full-scale ADC range = maximum signal power level + losses + RF/IF gain, or $0 \text{ dBm} = -13 \text{ dBm} - 6 \text{ dB} - 6 \text{ dB} + \text{gain}$. Therefore, you need a gain of 25 dB.

Distribute the 25-dB gain between the RF and IF stages (Figure 5). With a full-scale GSM signal at -13 dBm, the ADC input is 0 dBm. However, with a minimum GSM signal of -104 dBm, the signal at the ADC is -91 dBm.

Next, use these numbers to determine the suitability of the ADC in noise performance and spurious performance, looking at the amplifier and mixer specifications when the full-scale signal of -13 dBm drives their inputs. Solving for the third-order products in signal full-scale,

INPUT INTERCEPT POINT =

$$1.5 \text{ SIG} - \frac{3\text{OP}}{3} \text{ dB}$$

where SIG is the full-scale input level of the stage in decibels referred to 1mW, and 3OP is the required third-order-product level.

Assuming that overall spurious performance must be greater than 100 dB (to represent AMPS and CDMA require-

ments), the above equation shows that you need a third-order input amplifier with an IP3 greater than 37 dBm. At the mixer, the signal’s level increases by a 10-dB gain, and the new signal level is -3 dBm. However, specifying mixers at their output reduces this level by at least 6 dB to -9 dBm. For the mixer, you need an IP3 greater than 41 dBm. At the final gain stage, the signal is attenuated to -9 dBm. For the IF amplifier, you need an IP3 that is greater than 41 dBm.

ADC CLOCK JITTER

One dynamic specification that is vital to good radio performance is ADC clock jitter. Although low jitter is important to excellent baseband performance, sampling higher frequency signals (higher slew rates), such as the signals in undersampling applications magnifies low jitter’s effect. A poor jitter specification reduces SNR as input frequencies increase.

Texts frequently interchange the terms “aperture jitter” and “aperture uncertainty.” In this application, they have the same meaning. Aperture uncertainty is the sample-to-sample variation in the encoding process, and it increases system noise, causes uncertainty in the phase of the sampled signal, and causes intersymbol interference.

IF sampling typically requires an aperture uncertainty of less than 1 psec to achieve required noise performance. In phase accuracy and intersymbol interference, the effects of aperture uncertainty are small. In a worst-case scenario of 1-psec-rms uncertainty, the phase uncertainty, or error, is 0.09 rms at an IF of 250 MHz. This value is acceptable even for a demanding specification, such as GSM.

At a given frequency, f , the maximum slew rate occurs at the zero crossing and equals the peak signal amplitude $\times 2\pi f$. The units of slew rate are volts per second, indicating the signal’s speed as it slews through

at the zero crossing of the input signal.

In a sampling system, you use a reference clock to sample the input signal. Any sample-clock-aperture uncertainty results in an error in the sampled-signal accuracy. By multiplying the input slew rate by the jitter, you can determine this error voltage. You usually express aperture uncertainty in seconds rms and error voltage in volts rms. As the analog input frequency increases, the rms error voltage also increases for a constant aperture uncertainty.

Clock purity is important in IF sampling converters. As in mixing, a local oscillator (in this case, a sampling clock) multiplies the input signal. Because the multiplication in the time domain equals the convolution in the frequency domain, the spectrum of the sample clock is convolved with the spectrum of the input signal. Aperture uncertainty, which appears on the clock as wideband noise, also shows up as wideband noise in the sampled spectrum. Because the ADC is a sampling system, this spectrum is periodic and repeated around the sample rate. The wideband noise degrades the ADC's noise-floor performance. You can determine aperture uncertainty, which limits the theoretical SNR for an ADC, by:

$$SNR = -20 \log \left[\epsilon_{PF} F_{ANALOG} t_{j_{rms}} \right]$$

where F_{ANALOG} is the analog input frequency and $t_{j_{rms}}$ is the aperture uncertainty.

If you evaluate this equation for a 201-MHz analog input and 0.7-psec-rms jitter, which are typical for a high-performance ADC, such as the AD6640, you find that the theoretical SNR is limited to 61 dB. This SNR is the same one you need if you use another mixer stage. Therefore, systems that require very high dynamic range and very high analog input frequencies also require very low jitter in their encode circuitry. Standard TTL/CMOS clock oscillator modules can provide 0.7 psec rms; low-noise modules can provide better numbers.

When you consider overall system performance, use a more generalized equation. The following equation builds on the equation above but includes the effects of thermal noise and differential nonlinearity:

$$SNR = -20 \log \left[\frac{\epsilon_{PF} F_{ANALOG} t_{j_{rms}}}{\epsilon_{NL}} \sqrt{\frac{1 + \epsilon_{NL}^2}{2^N} + \frac{V_{NOISE_{rms}}}{2^N}} \right]$$

where F_{ANALOG} is the analog IF, $t_{j_{rms}}$ is the aperture uncertainty, ϵ is the average differential nonlinearity of converter (approximately 0.4 LSB), $V_{NOISE_{rms}}$ is the thermal noise in least significant bits, and N is the number of bits.

Although this equation is simple, it provides considerable insight into what noise performance you can expect from a data converter. You can find more details on aperture jitter in **Reference 2**.

PHASE NOISE

Although synthesizer phase noise is similar to jitter on the encode clock, it has slightly different effects on the receiver. The primary difference between jitter and phase noise is that jitter is a wideband problem with uniform density around the sample clock, and phase noise is a nonuniform distribution around a local oscillator and usually improves as you move farther away from the tone. As with jitter, less phase noise is better for your system.

When the local oscillator mixes with the incoming signal, noise on the local oscillator affects the desired signal. Phase noise from the local oscillator causes energy from adjacent and active channels to become integrated into the desired channel as an increased noise floor; this event is called "reciprocal mixing." To determine the amount of noise in an unused channel when a full-power signal occupies an alternate channel, you can use this GSM analysis:

$$NOISE = \int_{f=-0.1}^{+0.1} x(f) * p(f) df,$$

where noise is the noise in the desired channel caused by phase noise, $x(f)$ is the phase noise expressed in nonlog format, and $p(f)$ is the spectral density function of the Gaussian-filtered minimum-shift-keying function.

For this example, assume that the GSM signal power is -13 dBm. Also, assume that the local oscillator has a constant phase noise across frequency. (The phase noise often reduces with carrier offset.) Under these assumptions, when you integrate this equation over the channel bandwidth, you get the simple equation below. Assuming that $x(f)$ is constant and the integrated power of a full-scale GSM channel is -13 dBm, the equation simplifies to:

$$NOISE = PN \cdot SIGNAL_{ADJACENT}$$

or in log form,

$$NOISE = PN_{log} + SIGNAL_{log};$$

$$NOISE = PN + (-13 \text{ dBm});$$

$$PN_{REQUIRED} = NOISE - (-13 \text{ dBm}).$$

Your goal is to require phase noise to be lower than thermal noise. If you assume that noise at the mixer is the same as noise at the antenna (-121 dBm), then you can use noise in a 200-kHz GSM channel bandwidth at the antenna. Thus, the phase noise from the local oscillator must be lower than -108 dBm, with an offset of 200 kHz.

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