

**YOU CAN OFTEN TRACE THE DIFFERENCE BETWEEN A POWER SUPPLY THAT PRODUCES A STEADY, CLEAN, AND QUIET OUTPUT AND ONE THAT PRODUCES NOISY, UNRELIABLE POWER DIRECTLY TO THE SUPPLY'S BOARD LAYOUT.**

# Board layout boosts power-supply performance

**E**XPERIENCED POWER-SUPPLY designers employ a different set of guidelines from those most digital and analog designs use. Digital designers usually line up components in neat, logical rows, and the traces on the board are often as narrow as 6 mils. This method may produce an aesthetically pleasing digital design, but a similarly designed power supply probably does not function very well.

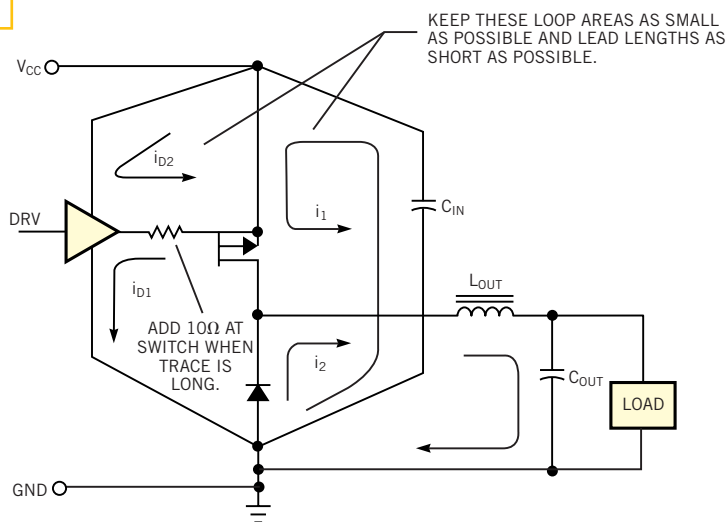
Many analog designers begin by laying out those portions of the design that are most likely to pick up interference. Then, they work outward from the sensitive nodes toward the design's output. Again, this method may work well for an analog design, but power-supply layout design requires other considerations.

Another poor layout method—called the scatter method—is not limited to power supplies. Designers also use this method in faulty digital layouts and faulty analog layouts. Designers approach the scatter method with little planning; they scatter the components on the board and connect them according to the schematic. No matter what sort of board you are designing, this method is a terrible way to lay out a board. Not surprisingly, a power supply laid out by the scatter method will usually produce noisy and unreliable power.

## FIRST THINGS FIRST

Experienced power-supply designers first consider the power-generating portions of the layout—the source of noise and interference. Second, they consid-

**Figure 1**



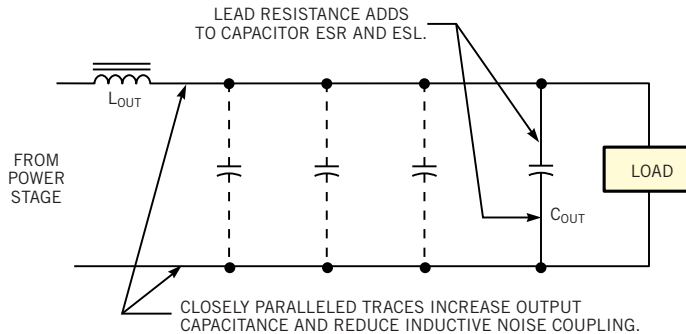
**The power stage is the main source of EMI in any power supply.**

er sensitive nodes in the layout that are susceptible to interference.

An efficient power-supply layout limits EMI and RFI by having small high-current loops, proper grounding of the control stage, and strategically sized traces to handle peak currents. Properly positioned ground planes can help, but controlling current flow is of the utmost importance. Small current loops achieve two things: They generate less radiation, and they produce less magnetic coupling between adjacent circuitry.

A strategic cut on a top-surface ground plane will control the electrical flow of output currents as well as currents in the power supply's control section. Other factors that contribute to an effective power-supply layout are the use of proper components; separation of the ground plane to reduce cross-conduction; the use of snubbers on the commutation and output rectifiers; and the strategic placement of components, which suppresses EMI and thus reduces noise-generation and pickup.

**Figure 2**



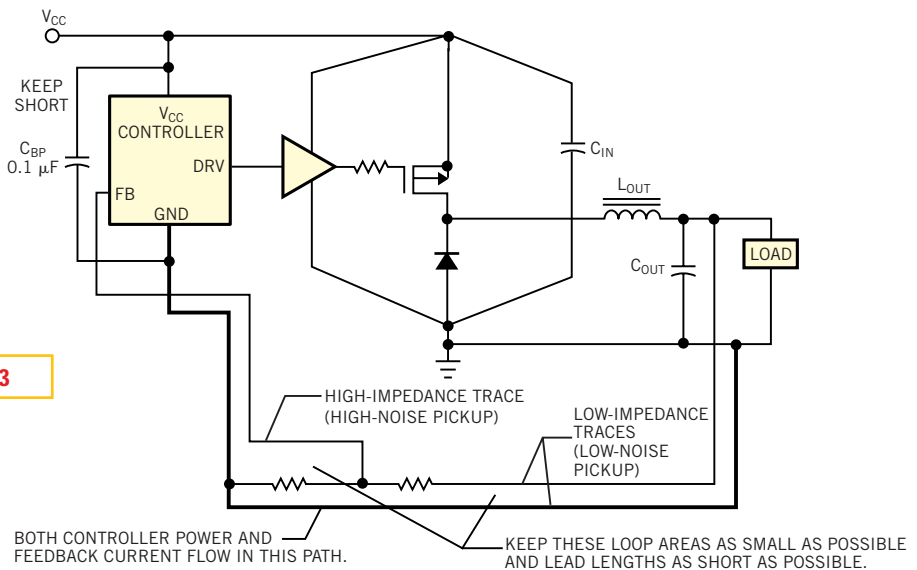
Parallel traces and short leads help in the output stage.

**THE POWER STAGE: A SOURCE OF EMI**

The first place to look for electrical noise is in the supply's power stage. This portion of the layout features the highest circulating currents and is therefore one of the main sources of EMI. Of primary concern is the size of the loops in the power stage's switching mechanism and drive circuit.

In a typical power stage, the input current flows through the input capacitor, the power switch, and the inductor before splitting between the output capacitor and the load (Figure 1). The inductor discharge or commutating current flows through the commutating diode and the inductor, and then flows to the output capacitor and the load. By placing the input capacitor, power switch, diode, and inductor as close together as possible, the loop areas of these current flows are kept to a minimum, and the circuit produces less EMI.

**Figure 3**



The controller stage is very sensitive to noise pick-up.

traces in the drive circuitry generate considerable RFI. As a rule of thumb, if the gate lead trace measures longer than approximately 2 in., you should place a small, approximately 10Ω resistor in the trace near the switch to reduce RFI.

**OUTPUT STAGE: HEAVY CURRENT**

In the output stage, heavy currents flow from the inductor, to the output capacitors, and eventually on to the load (Figure 2). The power trace and return trace in the output stage should be as close together as possible to minimize the loop area between these two traces and to increase coupling capacitance. An ideal layout design for a multilayer board would have these two

traces on adjacent layers, one directly above or below the other. For single-layer boards, keep the power and return traces as close to parallel as possible.

You should also keep the length of the trace from the output capacitor to the main board output as short as possible to minimize the equivalent series resistance (ESR) and equivalent series inductance (ESL). ESR and ESL contribute to the power supply's output ripple. This current ripple flows through the inductor and the output capacitor to the load. Designers sometimes use parallel capacitors in the output filter to minimize voltage ripple in the load and to reduce the circuit's total resistance. However, you must take care in the layout to as-

sure that the first of the parallel capacitors does not overheat from conducting a ripple current that is higher than the current that subsequent capacitors in the series conduct. Several layout solutions, such as a star configuration or narrow traces that gradually widen as they move from the inductor to the load, help alleviate this condition.

## CONTROL STAGE: NOISE SENSITIVE

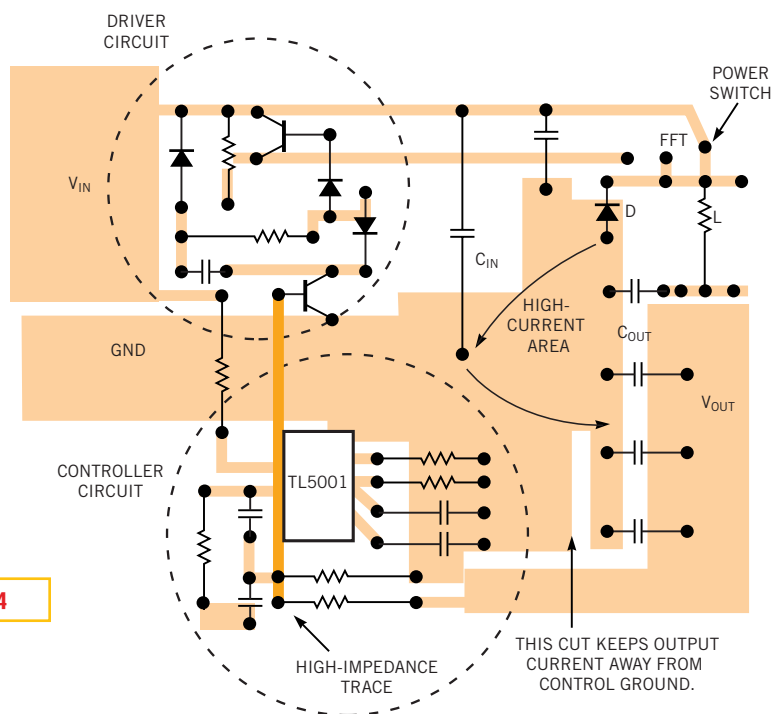
The power supply's controller section is very sensitive to noise pickup. Strategically placed ground connections can be critical to the performance of this stage.

Layout designers must carefully lay out the controller stage because any voltage difference between the grounds at the feedback-divider and the controller results in an error in the output voltage (Figure 3). Designers should ground the controller to its output ground so that the feedback divider is referenced to the controller ground. In addition, the operational amplifier amplifies any noise picked up by the sensing circuitry of the controller stage and feeds it directly to the output. To guard against this problem, the controller's supply current and feedback current should terminate in a single-point ground at the output.

To prevent the propagation of transient currents from the controller, you should place the bypass capacitor as close as possible to the controller. This bypass capacitor should have short leads to the controller's voltage supply ( $V_{CC}$ ) and ground pins. A surface-mounted capacitor laid out next to the controller provides the shortest possible routing.

In the controller stage, use parallel traces to reduce the area of current loops and minimize noise pickup and radiation. The feedback path from the low-impedance output through the resistor divider is not as critical as the path from the divider to the high-impedance op-amp inputs. The path from the divider to the error amp should be as short as possible and consist of parallel paths to reduce noise pickup. Breaking the ground plane into two or more sections with a single connection point can sometimes help keep the high output-return current from flowing around or near the controller circuit. This method can greatly reduce the amount of noise that the sensitive controller circuitry picks up.

Developing a layout for an effective power supply often involves trade-offs. For ex-



**Figure 4**

Proper board layout increases power-supply efficiency.

ample, you typically place the driver circuit as close to the power switch as possible. In the example layout shown in Figure 4, the shape of the board prevents the designer from placing the driver circuit and the input capacitor next to the power switch. Because the input capacitor circulates higher currents than the driver circuit, the designer correctly places the input capacitor adjacent to the power switch. As this example illustrates, you should use tight loops where currents are highest, such as in the loop from the input capacitor, throughout the clamp diode, and in the output capacitors, to reduce the electrical noise that the circuitry generates. The cut in the ground between the output capacitors and the controller keeps output return currents from flowing into the controller section of the layout, thus reducing noise and load-induced regulation errors.

The junction of the output divider resistors and the input pin of the controller is a high-impedance junction. As such, it is susceptible to noise pickup. In Figure 4, this junction is very short and as far as possible from noise-generating elements. A long trace at the top of the divider resistor does not jeopardize the efficiency of the layout because this point is low in imped-

ance and not tremendously sensitive to noise pickup.

Unlike many digital and low-level analog circuits, power-supply circuits handle a broad range of currents, from microamperes to 10s and even 100s of amps. Consequently, power-supply circuits can produce high-frequency signals that cause many problems within the load or the power supply itself if you don't handle them properly. By using proper board-layout practices, you can avoid many of the problems that power supplies commonly encounter. □

## Author's biography

Philip D Rogers is a systems engineer in the semiconductor division at Texas Instruments (Dallas). He received his BSEE degree from Southern Methodist University (Dallas). During his four years with Texas Instruments, he has worked on PWM controllers, low-dropout regulators, and MOSFET drivers. His current job concerns power-supply designs and laying out power-supply evaluation boards.