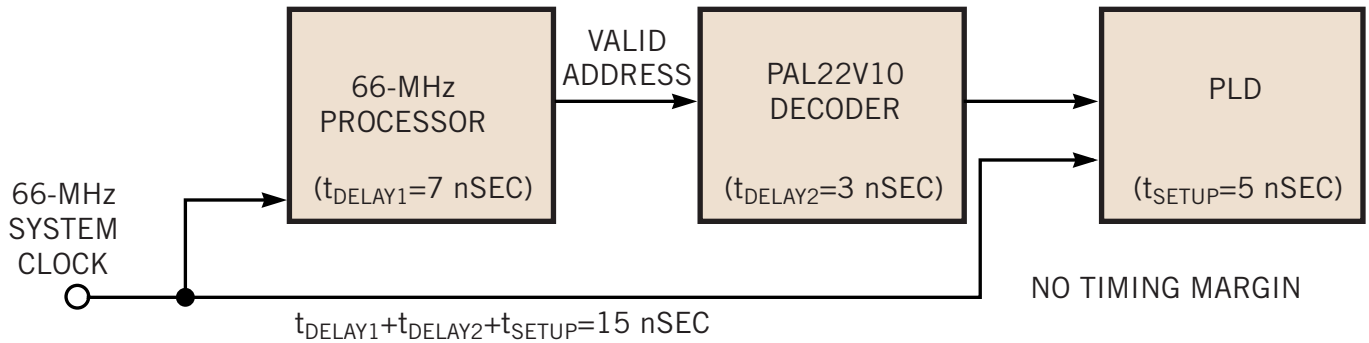
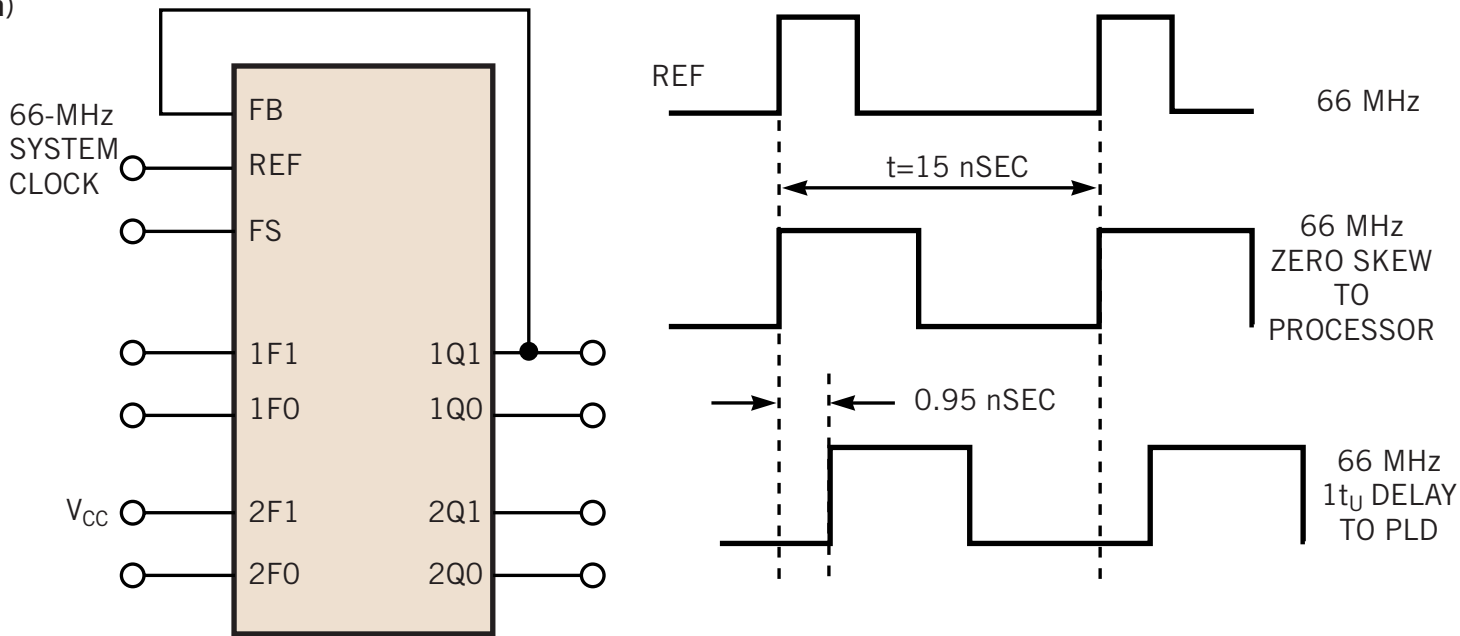


Figure 1



(a)



(b)

0.95 nSEC OF TIMING MARGIN

A programmable-skew clock driver has many uses, including dealing with device timing violations. To overcome a registered PLD's setup-time violation (a), the clock driver provides 0.95 nsec of timing margin (b).