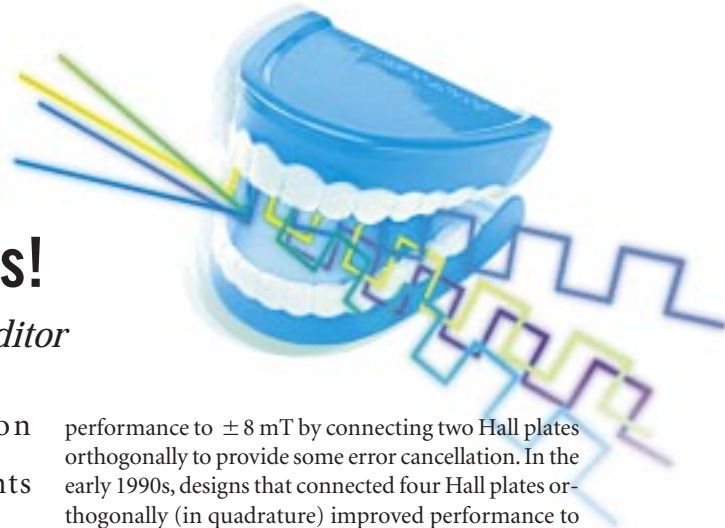


how it works

CMOS CIRCUITRY, NOTORIOUS FOR LOUSY ANALOG PERFORMANCE, PROVIDES ERROR-CANCELING CHOPPER TECHNIQUES TO DELIVER STERLING ANALOG PERFORMANCE.

Nice set of choppers!

Bill Travis, Senior Technical Editor



It seems almost an oxymoron that you can use circuit elements that deliver the lousiest analog performance known to designerkind to produce some of the best analog performance known to designerkind. Indeed, CMOS circuitry is

notorious for its poor linear performance in offset and drift, nonlinearity, and noise. However, CMOS transistors make near-ideal switches, and you can exploit the switches in chopper circuitry to provide stabilization, compensation, and error cancellation in linear circuits. Intersil (RIP) and Teledyne Semiconductor (now Telcom Semiconductor, www.telcom-semi.com) were early pioneers in chopper-stabilized op amps. References 1, 2, and 3 briefly describe the chopper techniques that Hall-effect sensor ICs use; here, we delve a little more deeply into the marvels of mixing digital and analog techniques.

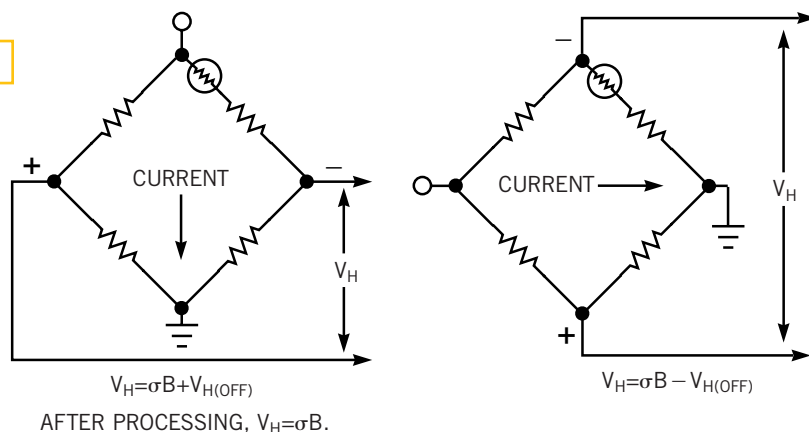
First, a little background in Hall-sensor technology might prove edifying. A Hall-effect sensor plate develops a voltage orthogonal to the direction of current flow when a magnetic field impinges on it. Hall-effect ICs in the 1970s used a single Hall plate with relatively terrible yields and performance. Stress-induced Hall-plate offset error was on the order of ± 25 milliteslas (mT). Designs in the 1980s improved the

performance to ± 8 mT by connecting two Hall plates orthogonally to provide some error cancellation. In the early 1990s, designs that connected four Hall plates orthogonally (in quadrature) improved performance to ± 4 mT. Good specs, but, unfortunately, the orthogonal error cancellation did nothing to cancel temperature drift. Expansion/contraction stresses in packaging produced totally random, unpredictable, and non-tracking drifts in the four Hall plates. The costly result was poor yields in temperature testing and binning.

CHOPPERS COME TO THE RESCUE

In 1994, CMOS-based chopper-stabilization techniques entered the scene. Figure 1 illustrates the technique for eliminating stress-induced Hall-plate offsets. The scheme uses floating CMOS switches to flip the quadrature-connected Hall plates' current source and the output connections by 90° . The resulting outputs for the two phases are then $\sigma B + V_{H(\text{off})}$ and $\sigma B - V_{H(\text{off})}$.

Figure 1



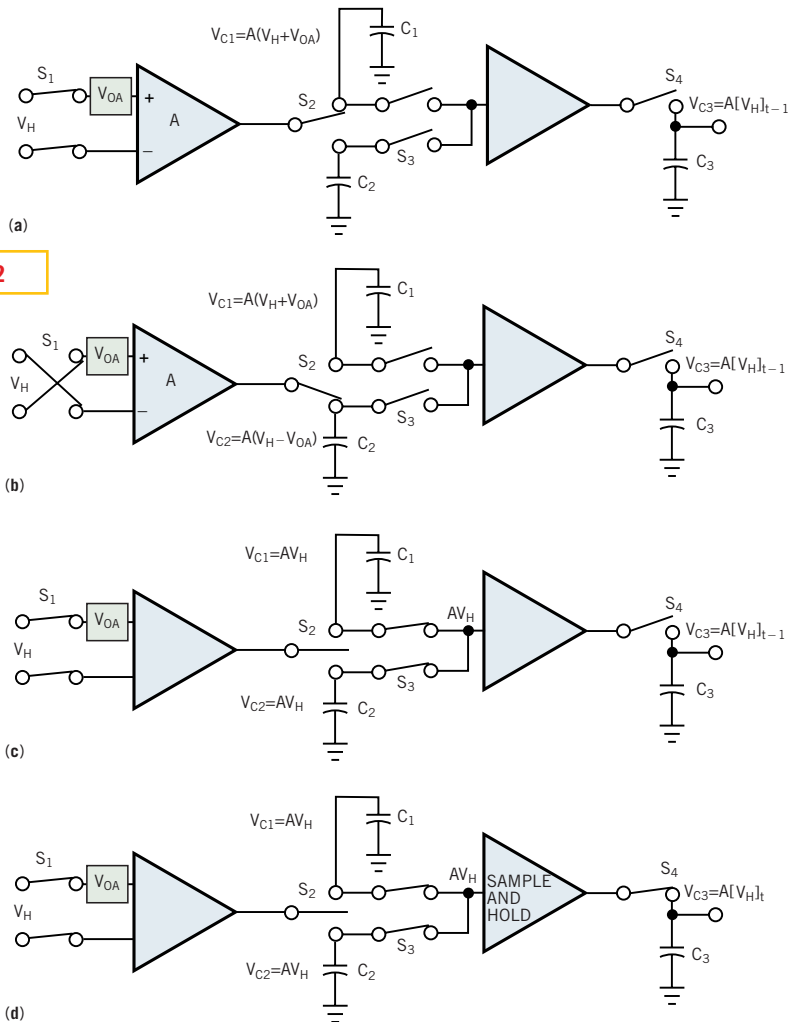
Flipping the connections of a quad Hall plate by 90° causes the strain-induced offset voltage to appear with alternating polarities at the output; subsequent demodulation removes the offset error.

It's a relatively easy task to demodulate the resulting waveform and provide lowpass filtering to eliminate the stress-induced Hall-plate offset, $V_{H(off)}$. This chopper scheme reduces Hall offset (and, especially, offset temperature drift) to more than two orders of magnitude lower than the offset of an unswitched quad configuration.

Given this clean, magnet-induced Hall-effect signal, the next step is to amplify the low-level signals to a useful level. As stated, CMOS circuitry makes poor linear amplifiers. With an amplifier gain of more than 100, the several-millivolt offset error of a CMOS op amp would swamp any useful Hall-effect signal. You can use laser trimming—zapping links or fuses—to null the offset voltage but, again, the nulling is valid only at 25°C. Moreover, laser trimming is an additional, cost-producing step in production. The same drawbacks, plus yield-loss costs, apply to selection, or binning, for low-offset parts. Again, chopper techniques come to the rescue. **Figure 2** shows the clever solution Melexis (www.melexis.com) uses. The circuit uses a four-phase switching scheme to eliminate the amplifier's offset error.

Phase 1 (**Figure 2a**) samples the positive offset ($+V_{OA}$) by charging C_1 through S_2 with S_1 in the position shown. By reversing the connections of S_1 , Phase 2 (**Figure 2b**) charges C_2 with the negative value of V_{OA} . (Not shown to avoid clutter, an additional switch inserts a unity-gain inverting amplifier in the signal path to C_2 in Phase 2, to restore the polarity of the flipped V_H and invert the polarity of V_{OA} . The offset error of this unity-gain block is negligible compared with the greatly amplified V_{OA} . That's the beauty of CMOS: You can sprinkle switches everywhere.) In Phase 3a (**Figure 2c**), S_2 connects C_1 and C_2 , the opposite-polarity V_{OA} voltages cancel, and only Hall-effect signal V_H remains on the capacitors. Phase 3b (**Figure 2d**) closes S_4 to update the output sample-and-hold capacitor C_3 with the latest Hall-effect signal. The chopper cycle creates a delay, or latency, equal to the duration of the three phases.

Mixing digital and analog techniques makes eminent sense in sensor ICs. Without such techniques, it would be virtually impossible to produce high-performance, cost-effective sensors with reasonable production yields. This statement is especially valid in automotive applications, which demand MIL-standard performance over outlandish temperature ranges at subcommercial prices. In addition to chop-



Clever use of CMOS switches makes it possible to cancel out the offset voltage in the high-gain input amplifier, leaving only the useful Hall signal at the output.

per techniques, Hall-sensor producers borrow other amenities from the digital world to add yet more functionality to their ICs. Melexis, for example, adds PROMs and D/A converters to its MLX90215VA linear Hall-effect sensor to allow you to program magnetic sensitivity and temperature coefficient, among other parameters. □

References

1. "Hall Effect IC Solutions," 1998 Catalog, Melexis Inc, pg 53.
2. Travis, Bill, "CMOS tricks stabilize Hall-effect sensor," *EDN*, Sept 1, 1997, pg 22.
3. Travis, Bill, "Hall-effect sensor has programmable everything," *EDN*, Jan 1, 1998, pg 12.