



leading edge

What's hot
in the
design
community

Edited by
Fran Granville

WRONG NUMBER?

"How do you deal with a 30-year-old phone system designed for three-minute conversations when people are using it to transfer graphics on the Internet for hours at a time?"—Mike Ricci, vice president of Level One Communications, on the problem of upgrading the communications infrastructure to give everyone all the bandwidth they need.

New processor architectures prevail

By Markus Levy

Fall brought a flurry of new processor architectures that continues to debut. Hitachi, Motorola, and QED are now providing offerings for the market for embedded systems (see "Fall brings

a flurry of processors," *EDN*, Oct 22, 1998, pg 11).

QED continues its MIPS-architecture evolution with the introduction of its RM5700, or

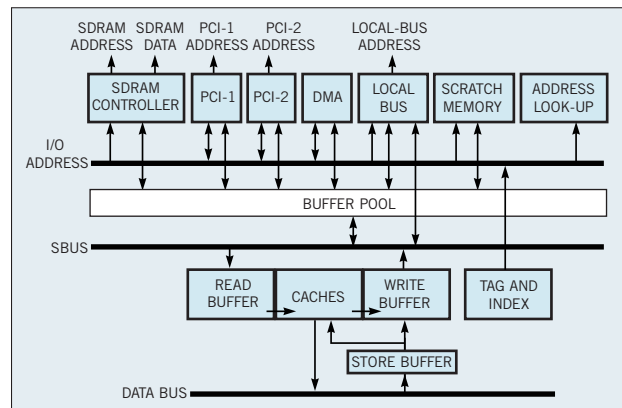
Alpine, embedded-processor family. The RM5700 family features a split internal-bus structure. The MIPS standard internal bus, which QED used in

previous designs, multiplexes the address and data bus. The split-bus structure allows the core to start a new address cycle during every CPU cycle. To prevent bus-throughput bottlenecks, QED implements a buffer pool—a cross between a multiported register file and a crossbar switch. The buffer size is 512 bytes, or 16 cache lines, and multiple masters on the RM5700's internal bus can simultaneously send data to the buffer. The multiported nature of the buffer pool eliminates the need for masters to arbitrate bus bandwidth.

The Alpine family is QED's first stab at integrating peripherals to target processors toward specific markets, such as networking and printers. The peripherals include a memory controller, PCI support, and DMA. The RM5700 uses a user-programmable address-look-up mechanism, similar to a content-addressable memory (CAM), to allow you to relocate these peripherals.

The memory controller supports a 64-bit interface and four external banks; it comprises three state machines and a command serializer that allows RM5700 devices to support three outstanding requests. RM5700 devices support a low-voltage-TTL interface as fast as 100 MHz and a stub-series-terminated transceiver-logic interface as fast as 133 MHz.

The memory controller allows you to prioritize PCI op-



QED's RM5700 family features a split internal-bus that allows the core to start a new address cycle during every CPU cycle.

Vendor firms up price of "ultimate" ADC

When *EDN* reported on National Instruments' announcement of a flexible-resolution ADC board that makes 8-bit conversions at 100M samples/sec and provides 160-dB spurious-free dynamic range at 100k samples/sec the company did not have firm pricing (see "PCI and CompactPCI boards sport 'ultimate' ADC," *EDN*, Sept 24, 1998, pg 20). The company has now established a firm price: \$3495. Initial shipments, during the first quarter of 1999, will be of boards in the "desktop" PCI form factor. The company has announced neither prices nor delivery of a CompactPCI version.—by Dan Strassberg

► **National Instruments**, Austin, TX. 1-800-258-7022, fax 1-512-683-8411, www.natinst.com. © Circle No. 433

erations before all others. In a printer application, for example, assume that the print engine stores a rasterized page in synchronous DRAM (SDRAM). It then becomes the system's highest priority to move the data from memory through PCI to avoid gaps on a page, even at the expense of a CPU stall during a cache miss. The memory controller can also leave 16 SDRAM pages open after use.

The first two devices in the RM5700 family include the RM5710 and RM5730, implementing single and dual PCI buses, respectively. Instead of implementing a standard CAM approach for translating PCI addresses, QED's RM5700 uses a type of memory-management unit (MMU). The MMU includes a translation-look-aside buffer with attribute fields. This approach allows you to set up a single PCI-based device with different priorities.

Hitachi's SH-DSP, containing an SH-2 core, tightly merges a CPU with a DSP. In the SH-DSP, the DSP unit shares the five-stage pipeline with the integer unit, and the CPU contains a fetch-and-decode unit, which manages the instruction stream for both the integer and the DSP units. The SH-3 DSP beefs up the performance of the SH-DSP and includes data-protection and virtual-memory functions using an MMU.

SH3-DSP uses a bit in the Control Register to turn on the DSP unit. On the SH-DSP, you

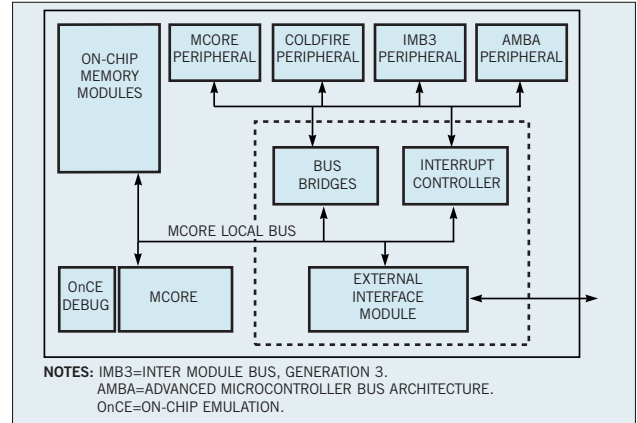
could access the DSP through the instruction stream. Whereas the SH-DSP has X, Y, and instruction buses, Hitachi adds a fourth bus to the DSP unit of the SH3-DSP. This fourth bus, the L bus, runs at the same frequency as the CPU. With this L bus, the DSP unit can perform a background DMA operation while the other buses access two data operands and one instruction.

The SH3-DSP has a unified 16-kbyte, four-way set-associative cache. It also has 16-kbytes of X/Y memory in an unmapped address space. Hitachi has added an auxiliary data port (AUD) that allows the company's debugging hardware to track execution branches. The chip uses a Hitachi-patented compression method to send the source and destination addresses of branches out over the AUD port. The AUD can operate in a real-time mode during which the processor continues to run at full speed even if the AUD port's FIFO buffer overflows. A full-trace mode, although not real-time, stalls the processor.

Hitachi's first standard product based on the SH3-DSP architecture is the 133-MHz SH-7729, which consumes 200 mW at 1.8V and comes in a 216-pin chip-scale package or 208-pin low-profile QFP. In addition to the DSP unit, the SH7729 chip has the same peripheral modules as the SH7709 (SH-3) but with a larger cache and emulator support.

Meanwhile, enhancing its MCore line, Motorola has added the M300, the superpipelined M500, and the superscalar M600 families. The M300 targets applications needing floating-point and numeric acceleration. The company based the core on the M210 core but added support for single-precision floating-

parallel, effectively reducing load/store instructions to one clock. The M300 also supports bus arbitration and branch folding. When the M300 detects a backward branch, it replaces the branch instruction with the instruction that the loop address points to, saving two cycles for each pass through the loop.



Motorola offers several modules that provide the link between the MCore local bus and MCore, ColdFire, 68300, or ARM peripherals.

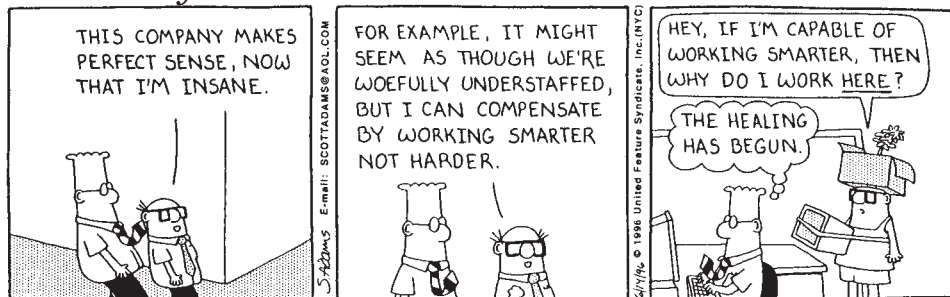
point and fast-multiply operation. Motorola also added a 32-bit, dual-instruction-prefetching feature that allows the core to simultaneously fetch two 16-bit instructions. A 16-bit instruction buffer helps reduce external-bus accesses; the M300 can store as many as four instructions in an internal two-level buffer.

Load/store instructions in the MCore architecture require two clocks. The M300 performs data-dependency checking and allows nondependent load/store instructions to execute in

As its name implies, MCore is available as an embeddable core. To help you interface peripherals to MCore, Motorola offers several modules that provide the link between the MCore local bus and MCore, ColdFire, 68300, or ARM peripherals. Motorola calls this module the Peripheral Interface Gasket (PIG)-interrupt external-interface (PIE) module. The PIE module contains an interrupt controller that can operate in MCore or 68K-like modes. The interrupt controller passes the vector to the core as the interrupt is occurring, improving determinism.

- ▶ **Hitachi America**, Brisbane, CA. 1-415-589-8300, www.hitachi.com/semiconductor. © Circle No. 434
- ▶ **Motorola**, Austin, TX. 1-800-441-2447, www.mot-sps.com. © Circle No. 435
- ▶ **Quantum Effect Design Inc** Santa Clara, CA. 1-408-565-0300, www.qedinc.com. © Circle No. 436

DILBERT By Scott Adams



ITC '98: Business is down; cooperation is up

At last month's International Test Conference (ITC) (www.itctestweek.org) in Washington, the automatic-test-equipment (ATE) industry was in one of its worst downturns in recent

memory. Orders had fallen by almost two-thirds from the spring of 1997's frenetic pace.

With these sobering economics as a backdrop, the technological forecasts took on an air of realism that was missing in the more rarefied atmosphere of the last few ITCs. Gone were claims that built-in-self-test (BIST) was a panacea that would do away with ATE as we know it. Gone too, were the pious proclamations that we, our children, and their children would never see useful BIST in our lifetimes.

In the era of systems on chips (SOCs), a new spirit of cooperation among ATE and BIST suppliers seemed to be emerging. Some ATE manufacturers acknowledged that using BIST to test complex ASICs' embedded-memory structures could make sense. In fact, Credence Systems (www.credence.com) and LogicVision (www.logicvision.com) announced an alliance to develop ATE optimized for devices that contain BIST structures and BIST structures optimized for compatibility with ATE. Cre-

dence also announced a technique that it calls BOST (built-off-chip self-test) for cost-sensitive ICs that can't afford BIST's chip-area penalties. Using BOST, test circuitry embodied in special devices resides on the load board that interfaces the device under test to the ATE system. Credence developed BOST with the cooperation of a leading supplier of computer-graphics ICs. That company tests its ICs on Credence testers.

Several ATE companies indicated that SOC ATE systems have to do everything. SOC chips embody many types of circuits—from logic to memory to mixed signal to RF. SOC testers must be configurable to handle all of them. Yet the configurability must not impose cost penalties unless a feature is present. The prototypes for such testers appear to be today's mixed-signal ATE systems. Mixed-signal testers have long been highly configurable with a wide variety of options.

Aside from SOC ICs, the most likely driver for the ATE indus-

try's next turnaround is direct Rambus dynamic RAM (RDRAM), which IC manufacturers produce under license from Rambus Inc (www.rambus.com). Intel Corp (www.intel.com), the leading supplier of microprocessors and peripheral chip sets and a major supplier of PC motherboards, says that RDRAM will be its future μ Ps' standard memory. The largest PC manufacturers say that they intend to build units that use RDRAM. All major memory-ATE suppliers claim to have systems that test RDRAM, which now interfaces via an 800-MHz serial bus and soon will run at more than 1 GHz. Several IC manufacturers are already offering RDRAM parts for sampling.

Other IC vendors are reportedly reluctant to pay royalties to Rambus and developing alternative high-speed memory parts. Intel competitors may design their μ Ps around such devices. Hence, the success of Rambus memory, though still likely, is not a sure thing.

Hewlett-Packard (www.hp.com/go/semiconductor), which heretofore has not been a major player in memory ATE, debuted an RDRAM tester at ITC. To develop its 95000 series of high-speed RAM testers, HP leveraged the technology of its successful 83000 series of high-speed logic testers. The 95000 can test all types of high-speed RAM. However, the designers had in mind the special requirements of single-pass testing of multiple RDRAMs in parallel. According to HP, besides highly advanced technology based on a tester-on-a-chip architecture, a major 95000-series selling point is the system's small size: It occupies one-third the floor area of competitive testers.

—by Dan Strassberg

PORT-BYPASS IC AVOIDS TRAFFIC JAMS ON DATA HIGHWAYS

For data rates as high as 2.5 Gbps, the S2091 port bypass IC from Applied Micro Circuits lets you switch between your normal connection and a bypass path, thus avoiding a failed or suspect node. You can use this 20-pin IC for applications such as 2.5 Gbps synchronous-optical-network (SONET) wavelength-division multiplexing (WDM), 2.1-Gbps Fibre Channel arbitrated-loop (FC-AL) disk-array, and 1.5-Gbps high-definition-TV broadcast-video designs. The 3.3V device typically dissipates 0.4W and includes 50 Ω source-terminated outputs. Its internal signal paths are fully differential to minimize jitter accumulation, a degradation that is a major concern at these high data rates.

You set the normal/bypass mode via a TTL select line in this \$41 (100) TSSOP IC.—by Bill Schweber
► Applied Micro Circuits Corp, San Diego, CA. 1-619-450-9333, fax 1-619-450-9885, www.amcc.com.

◎ Circle No. 437

EXPLOSIVE GROWTH FORECAST FOR USB

In 2002, nearly 400 million PC peripherals supporting the Universal Serial Bus (USB) will represent a market of more than \$1 billion, according to market-research company In-Stat. "USB will be the primary connection for human-interface ICs and peripherals," says Scott Hudson, senior analyst for Cahners In-Stat Group's PC Technology Service. "Because you can integrate USB technology into microcontrollers and other ICs, new competition with potential market shift will occur." In-Stat, 1-408-345-4455.

FACTOID► Seven people gain Internet access every second.

Keep your 2.5V ICs happy with 3.3V regulator's low dropout

As IC operating voltages drop to 2.5V from a 3.3V bus to save power, you have a challenge: The dropout voltage of the requisite regulator can be too great for reliable operation from a $\pm 10\%$ rail. Micrel's 1.5A MIC39150 and 3A MIC39300 low-dropout regulators overcome this problem, because they run from a 3.3V supply and give a 2.5V output even as

the supply rail drops to 3V. Besides basic low-dropout-regulator functions, these devices protect against reverse battery, current limiting, and thermal shutdown, and you can use them with supply voltages as high as 16V. These 1%-tolerance regulators are available in TO-220 and surface-mount TO-263 packages and cost \$1.56 and \$2.13 (1000), respec-

tively, for the 1.5A and 3A models. Enhanced versions of each include an enable-shutdown pin as well as an open-collector error-flag output, which signals when the output drops more than 5% below nominal value.

—by Bill Schweber

► **Micrel Inc**, San Jose, CA. 1-408-944-0800, fax 1-408-944-0970, www.micrel.com.

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SMART BATTERIES REAP BENEFITS OF ADVANCED IC SUPPORT

The potential benefits of smart battery packs don't come easy: To get the maximum potential from the pack, you need sophisticated electronics that let you apply advanced algorithms and to track cells. To help you achieve this potential, Powersmart Inc offers the P3 and P4 programmable smart-battery ICs. The SMBus-compliant P3 ICs have externally expandable nonvolatile-memory options; in contrast,



the P4 family members include on-chip flash EEPROM, and you can configure the devices for custom protocols and the I²C bus.

The 6 kbytes of memory in the P4 devices hold critical battery-management algorithms, cell-chemistry models, general and cell-specific calibration factors, related equations, and operating factors that the IC learns during operation. Both families have integrating 14-bit A/D converters with 1% accuracy, complex battery-cell models, and a RISC processor for data computation. The 28-pin SSOPs cost less than \$4 (OEM).

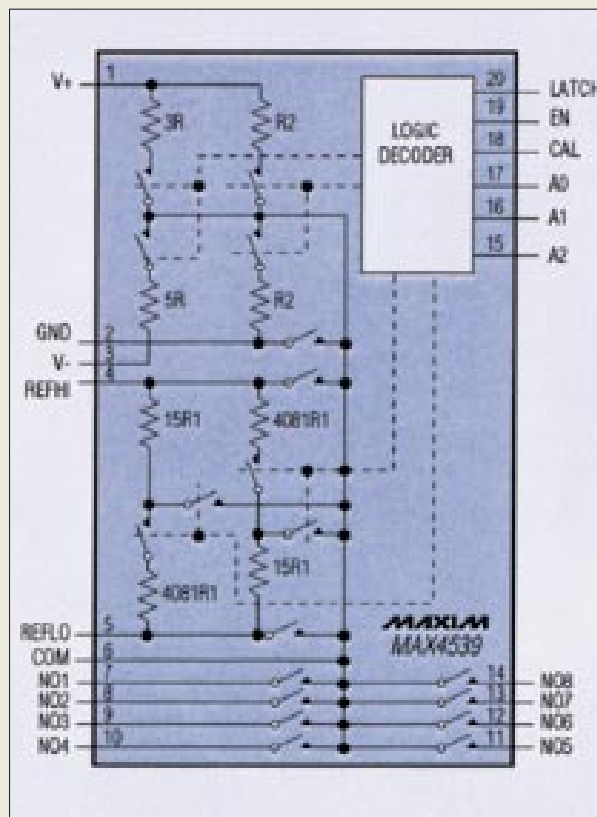
—by Bill Schweber

► **Powersmart Inc**, Shelton, CT. 1-203-925-1340, fax 1-203-925-1714, www.powersmart.com. ©Circle No. 440

Analog multiplexers eschew external calibration resistors

For calibration and self-monitoring of precision A/D-converter channels, designers often use voltage-divider resistor strings that connect to a reference. The eight-channel MAX4539 and dual four-channel MAX4540 multiplexers from Maxim save you the trouble, because they incorporate the needed precision resistors. You can switch inputs between $15/4096$ and $4081/4096$ division ratios of the external reference voltage (accurate to 15 bits), as well as between one-half the positive supply rail and five-eighths of the positive and negative supply rails (accurate to 8 bits). The multiplexers operate from a single-ended 2.7 to 12V supply or a ± 2.7 to $\pm 6V$ dual supply. Each device matches nominal 100 Ω maximum channel on-resistances to 6 Ω . Prices for these 20-pin ICs start at \$2.84 (1000).—by Bill Schweber

► **Maxim Integrated Products**, Sunnyvale, CA. 1-408-737-7600, www.maxim-ic.com. ©Circle No. 439



Toss away those external precision calibration resistors on your analog channels: Maxim's eight-channel MAX4539 and dual four-channel MAX4540 multiplexers include them within the IC and yield accurate fractional ratios of the external reference and supply rail voltages.

FACTOID► According to a PricewaterhouseCoopers study, venture capitalists put \$3.7 billion into start-up companies in the second quarter of 1998; 73% of the money went to 560 technology companies.

**BOOK KEEPS YOU
IN TOUCH WITH
TODAY'S PRODUCTS**

To explain how many common electronic products work, Philip Hoff, the author of *Consumer Electronics for Engineers* (Cambridge University Press, ISBN 0-521-58817-0) aims to fill the gap between simplified technical books that don't tell enough and trade publications that assume you know more than you do. The \$54.95 paperback book is also available in hard cover for \$110. It covers the circuits and systems of products such as AM and FM radios, audio tape recorders, monochrome and color TVs, VCRs, digital audio and CDs, and telephones.

Each chapter examines basic circuitry within the product and also explains the principles of operation, targeting engineers with a few years of experience. The book looks at critical parameters and trade-offs in design, using a mix of block diagrams, simplified schematics, key waveforms, and product schematics. The author doesn't talk down to you because he assumes that the audience is reasonably knowledgeable but wants to understand a design and how it functions at the micro (circuitry) and macro (system) level. *Consumer Electronics for Engineers* is the engineering equivalent of the popular *The Way Things Work* by David Macaulay. If you want to better understand the big and small picture, check out this book.—by Bill Schweber

Drive capacities vault 36-Gbyte barrier

As if they planned it, leading disk-drive vendors Fujitsu, IBM, Quantum, and Seagate rolled out new high-end product families exactly three weeks before Fall Comdex. Each of the rivals debuted

3.5-in., 1.6-in.-high models that top 36 Gbytes in capacity, and Seagate pushed the high end of its Barracuda line to 50 Gbytes. Moreover, the companies all have new 1-in.-high models with 9- and 18-Gbyte capacities. Fujitsu, IBM (UltraStar), and Seagate (Cheetah and Barracuda) all offer a choice of Ultra2 SCSI and Fibre Channel arbitrated-loop (FC-AL) interfaces, and IBM also offers Serial Storage Architecture (SSA) models. Quantum (Atlas IV and 10K) initially will offer Ultra2 SCSI models and next year will add FC-AL on the Atlas 10K family.

Most of the new drives feature 7500- to 10,000-rpm spin rates that have dropped average seek times to approximately 5 msec and sustained transfer rates to around 30 Mbytes/sec. Fujitsu tops the transfer-rate specs with a peak rate of 45 Mbytes/sec. Fujitsu is also the only of the four to move exclu-

sively to giant magnetoresistive (GMR) heads that yet again up areal densities. Fujitsu is using GMR heads across its entire desktop, mobile, and enterprise product families, and the move resulted in a 6.5-Mbyte, 2.5-in. drive. IBM, meanwhile, did much of the pioneering work on GMR and also included the technology in its new 18-Gbyte Ultrastar 18ES workstation/desktop drive that spins at 7500 rpm. IBM stuck with magnetoresistive heads on its 10,000-rpm enterprise Ultrastar 18ZX and 9LZX products and the 7500-rpm, 36-Gbyte Ultrastar 36XP. All of these drives should hit the streets around press time, and pricing will be aggressive. For example, expect 7500-rpm, 9-Gbyte SCSI drives to sell for a list price of \$600 and 10,000-rpm models to sell for around \$750.

Specs are one thing, but the next few months should reveal the true winners among the

new drives. Most experts agree that GMR heads will be necessary for the industry to move forward, but any such transition is risky for each player. Move too late to a new technology such as GMR, and you won't have competitive products. Move too soon, and a lack of heads or high head prices can derail your product. Fujitsu claims it can take the GMR risk early because it manufactures its own heads. IBM and Seagate, meanwhile, have each previously shipped 10,000-rpm products, and they believe a more conservative transition is in order. Look for a comprehensive report on disk-drive technologies in the Jan 21, 1999, issue of *EDN*.

—by Maury Wright

► **Fujitsu**, San Jose, CA. 1-408-432-6333, www.fcpa.com.

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► **IBM**, San Jose, CA. 1-888-426-5214, www.ibm.com/hardrive. ©Circle No. 442

► **Quantum**, Milpitas, CA. 1-408-894-4000, www.quantum.com.

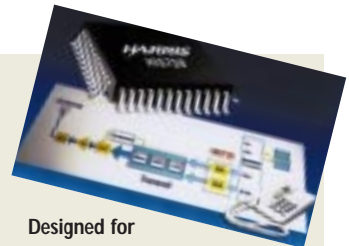
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► **Seagate**, Scotts Valley, CA. 1-408-438-6550, www.seagate.com. ©Circle No. 444

DUAL-CHANNEL DAC PUMPS WIRELESS APPS AT 125M SAMPLES/SEC

Many communications architectures use quadrature (I/Q) modulation and so need two channels of A/D or D/A conversion. The Harris Semiconductor HI5728 DAC offers 10 bits of resolution at a 125M-sample/sec update rate on each of its two closely matched channels—an additional virtue for I/Q systems. Spurious-free dynamic range is typically 75 dB at the maximum sampling rate for a 32.9-MHz output frequency; singlet (peak) glitch with a 25Ω load is 35 pV/sec. The 20.48-mA full-scale current-output IC includes an internal 1.2V reference and an input-data register. A 48-pin TQFP device, it uses either a 3 or 5V supply, consuming 165 mW per channel at the higher voltage and 54 mW per channel at the lower supply rail. The HI5728 costs \$14.08 (100).—by Bill Schweber

► **Harris Semiconductor**, Melbourne, FL. 1-800-442-7747, www.semi.harris.com. ©Circle No. 449



Designed for applications such as wireless local loops and multilevel quadrature-amplitude-modulation systems, in which I and Q channels must be closely matched, the Harris HI5728 dual-channel D/A converter accepts 10-bit updates at 125M samples/sec.

FACTOID► A first edition of Galileo's 1610 *Sidereus Nuncius* sold in June 1998 for \$380,000 at auction; you can now get the book as facsimile on CD ROM for \$25.

Crossbar bumps bandwidth to 1 Gbyte/sec

In the quest for the highest performance multi-computer systems, Mercury Computer Systems is about to take a giant leap with the introduction of the next generation of Race switched fabric archi-

tecture. Race++, an evolutionary enhancement, increases the aggregate bandwidth of Race crossbars from 480 Mbytes/sec to 1 Gbytes/sec.

The heart of Race++ is Mercury's new eight-port crossbar ASIC that increases the number of concurrent datapaths, along with a modest increase in data rates from 40 to 66 MHz. The Race++ architecture selects the

least congested datapath between source and destination in real time. This adaptive routing executes entirely in hardware and incurs no system or user-software overhead. Race++ also provides the determinism that real-time computing requires.

Race++ boosts the number of processors from the current Race architecture limit of 1000

processors to more than 4000 processors in one system. Race++ is also backward-compatible with the current Race architecture and the more than 60 products from third-party adopters of the industry-standard Raceway Interlink (ANSI/VME International Trade Association 5-1994).

Mercury anticipates the introduction of initial RACE++-based products in early 1999, with production shipments available in mid-1999.

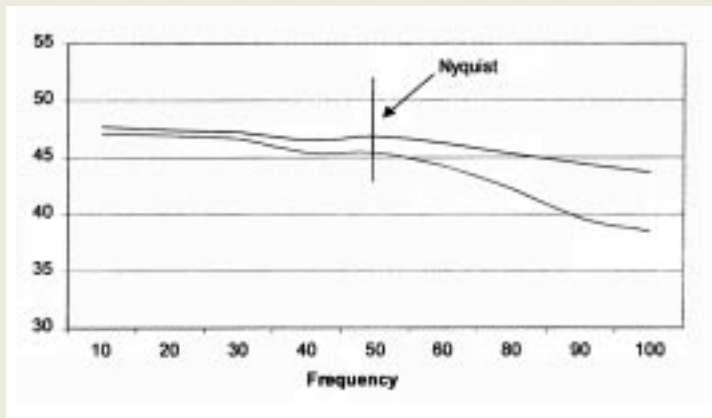
—by Warren Webb

► **Mercury Computer Systems Inc**, Chelmsford, MA. 1-978-256-1300, fax 1-978-459-8356, www.mc.com. ©Circle No. 445

100M-sample/sec ADC survives on 3V yet doesn't skimp on key specs

The AD9283 8-bit A/D converter from Analog Devices provides 100M-sample/sec conversions and operates from a 3V supply. The 20-pin SSOP IC includes onboard track/hold circuitry, an encoding clock, and an internal reference. Its performance optimizes SNR and SINAD (SNR and distortion) over a wide dynamic and frequency range. The device consumes 110 mW while sampling a 10.3-MHz analog input at full speed. Applications for this \$8.50 (1000) converter include camcorders, battery-powered instruments, and low-end digital oscilloscopes. —by Bill Schweber

► **Analog Devices Inc**, Norwood, MA. 1-781-937-1428, fax 1-781-821-4273, www.analog.com. ©Circle No. 446



The 8-bit AD9283A/D converter demonstrates high-performance SNR (upper trace) and SINAD (lower trace) for sine-wave inputs of 10 to 100 MHz at its maximum sampling rate of 100M samples/sec.

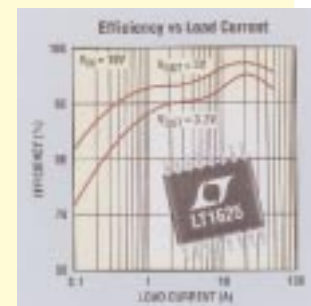
STEP-DOWN SWITCHING REGULATOR DELETES COMMON SENSE RESISTOR

By measuring voltage across the external MOSFET it is driving, rather than using the conventional but efficiency-draining method of sensing current via a resistor, the LTC1625 high-power current-mode controller from Linear Technology Corp achieves efficiency as high as 97% while optimizing efficiency at lighter loads. You can give the IC an input voltage of 3.7 to 36V; output voltage can be as low as 1.9V or as high as the supply. The controller provides synchronous drive for two N-channel MOSFETs and includes fold-back current-limit protection for these devices. You set the operating frequency of the LTC1625 at 150 to 225 kHz, or you can allow it to self-synchronize to an external clock. The 16-pin IC costs \$4.55 (1000).

—by Bill Schweber

► **Linear Technology Corp**, Milpitas, CA. 1-408-432-1900, fax 1-408-434-6441, www.linear-tech.com.

©Circle No. 447



The LTC1625 eliminates the need for an external sense resistor to measure inductor current; instead, it measures V_{DS} across the conducting MOSFET.

FACTOID► The decentralized World Wide Web is "governed" by the World Wide Web Consortium (W3C), which has 275 member organizations and is headed by Tim Berners-Lee, who invented the Web and URL scheme for linking documents while working at CERN (the European high-energy physics lab) in the late 1980s/early 1990s.

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Scan-rate converter eases move to HDTV without abandoning NTSC

In consumer applications, such as video, you have to look forward and backward at the same time. The SDA9400 scan-rate converter family from Siemens Microelectronics lets you maintain

backward compatibility of high-definition TV (HDTV) with the current standard by converting 50/60-Hz interlaced NTSC content into progressive-scan output, which the new standard needs, or 100/120-Hz interlaced images.

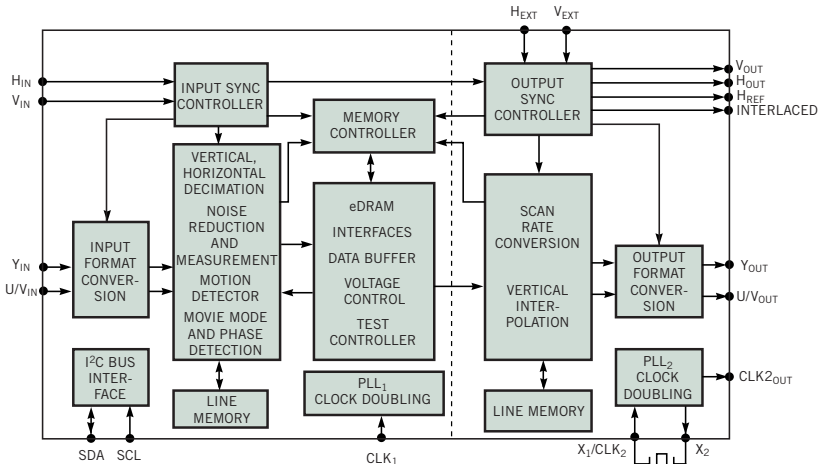
The SDA9400 devices increase the approximately 240

lines of the single field (half-frame) of an NTSC format to 480 lines to eliminate visible line structure on large-screen displays and takes image motion into account. The IC includes as much as 5.2 Mbytes of DRAM supported by a memory-synchronization controller; embedded algorithms that

identify, on a pixel-by-pixel basis, which method the device should use for scan-rate conversion and thus to minimize image artifacts; vertical and horizontal decimation for split-screen and double windows; and temporal and spatial noise-reduction circuitry. Other members of the family have similar features but support PAL format in addition to NTSC. The SDA9400 costs \$40 (10,000).—by Bill Schweber

Siemens Microelectronics Inc, Cupertino, CA. 1-408-777-4500, fax 1-408-777-4988, www.smi.siemens.com.

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The SDA9400 scan-rate converter lets your progressive-scan HDTV design maintain backward compatibility with the interlaced-scan NTSC format.

CALENDAR

NOV 30 TO DEC 4

Communication Systems Using Digital Signal Processing, Los Angeles, is a short course that emphasizes the application of modern DSP techniques to the implementation of communications systems. The course covers error-correction coding, spread-spectrum techniques, and bandwidth-efficient signaling. It also describes basic digital-signaling methods and modulation-with-memory techniques.

Registration costs \$1595 and includes course materials. Attendees should bring a calculator. UCLA Extension, Los Angeles, CA. 1-310-825-3344.

DEC 8 TO 9

Fundamentals of Electrical Distribution Systems, Boston, covers basic concepts of electrical systems, including voltage and current in ac and dc circuits; resistance, inductance, capacitance, and impedance; rms and average val-

ues; power in ac and dc circuits; three-phase systems; and more. Other topics include generation, transmission, and distribution; feeders, networks, and services; distribution-system components; electric fields; electrical machinery; system protection; load characteristics; power metering; system grounding; and power quality. The seminar is also available Dec 10 to 11 in Philadelphia, Jan 19 to 20 in Detroit, and Jan 21 to 22 in Atlanta. The seminar costs \$975. Educational Program Innovations Center, Dearborn, MI. 1-888-374-2338.