

ACCURATELY MEASURING THE SETTLING TIME OF A 16-BIT DAC AND ITS OUTPUT AMPLIFIER IS AN ART FORM. ONE MEASUREMENT TECHNIQUE BORROWS FROM THE DESIGN OF A CLASSIC SAMPLING OSCILLOSCOPE AND PROVIDES RELIABLE RESULTS. THREE OTHER MEASUREMENT APPROACHES PRODUCE RESULTS THAT CLOSELY AGREE WITH EACH OTHER.

Measuring 16-bit settling times: the art of timely accuracy

INSTRUMENTATION, WAVEFORM GENERATION, data acquisition, feedback-control systems, and other applications are beginning to make use of 16-bit data converters, specifically 16-bit DACs. By providing 16-bit performance at a lower cost than previous modular and hybrid technologies, new ICs make 16-bit DACs a practical design alternative. With the increasing use of these high-resolution devices comes an increasing need for techniques that accurately and reliably measure performance.

A DAC's dc specifications are relatively easy to verify; the measurement techniques are well-understood, although they are often tedious. The ac specifications, however, require more sophisticated approaches to produce reliable information. In particular, the settling time of a DAC and its output amplifier is extraordinarily difficult to determine to 16-bit resolution.

DAC settling time is the elapsed time from the input-code application until the output arrives at and remains within a specified error band around the final value. Manufacturers usually specify the settling time for a full-scale 10V transition. DAC settling time has three distinct components: During delay time, which is very small and almost entirely due to propagation delay through the DAC and output amplifier, there is no output movement; during slew time, the output amplifier moves at its highest possible speed toward the final value; and during ring time, the amplifier recovers from slewing and ceases movement within some defined error band (Figure 1). Normally, there is a trade-off between slew and ring time. Fast-slewing amplifiers generally have extended ring times, which complicate amplifier choice and frequency compensation. Additionally, the architecture of very fast amplifiers usually dictates trade-offs that degrade dc error terms (see sidebar "Practical consid-

erations for DAC-amplifier compensation").

It is difficult to measure to 16-bit ($\approx 0.0015\%$) accuracy regardless of the speed of what you are measuring. Dynamic measurement to 16-bit resolution is particularly challenging, and even more so if you use specialized components (see sidebar "Measuring the settling time of chopper-stabilized amplifiers"). A reliable 16-bit settling-time measurement requires exceptional care in your experimental technique. Accurate 16-bit results require careful attention to breadboarding, layout, and connection techniques. Wideband 100- μV -resolution measurements do not tolerate a cavalier laboratory attitude (Reference 1).

COMMON APPROACH OVERDRIVES OSCILLOSCOPE

A common circuit that you use to measure DAC settling time employs the "false-sum-node" technique (Figure 2). The resistors and DAC amplifier form a

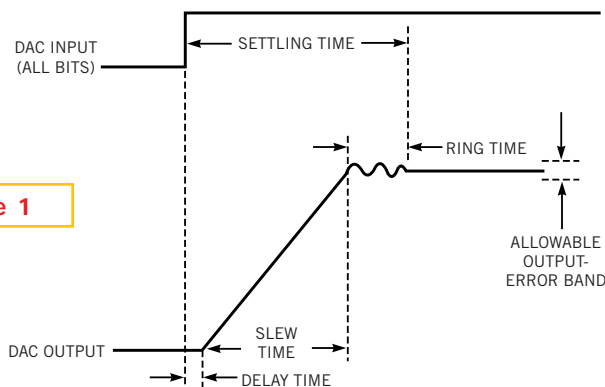


Figure 1

DAC-settling-time components include delay, slew, and ring times. Fast amplifiers reduce slew time, although longer ring time usually results.

bridge-type network. Assuming ideal resistors, the amplifier output steps to the value of V_{IN} when the DAC inputs move to all ones. During the slew time, the diodes bound the settle node, which limits the voltage excursion. When settling occurs, the oscilloscope probe's voltage should be zero. The resistor divider's attenuation means that the probe's output equals one-half of the actual settled voltage.

In theory, this circuit allows you to observe the settling to small amplitudes. In practice, this circuit does not reliably produce useful measurements. The oscilloscope connection presents problems. As probe capacitance rises, ac loading of the

resistor junction influences the observed settling waveforms. A 10-pF probe alleviates this problem, but its 10× attenuation sacrifices oscilloscope gain. 1× probes are unsuitable because of their excessive input capacitance. An active 1× FET probe works, but another issue remains. The clamp diodes at the settle node reduce swing during amplifier slew time and thereby prevent excessive oscilloscope overdrive. Unfortunately, overdrive-recovery characteristics vary among oscilloscopes, and vendors do not usually specify these characteristics (see sidebar “Evaluating oscilloscope-overdrive performance”). The Schottky diodes’ 400-mV

drop means that the oscilloscope may see an unacceptable overload and display questionable results.

At 10-bit resolution—10 mV at the DAC output or 5 mV at the oscilloscope—the oscilloscope typically undergoes a 2× overdrive at 50 mV/div, and the desired 5-mV baseline is barely discernible. At 12-bit or higher resolution, making a valid measurement using the circuit in **Figure 2** is hopeless. Increasing oscilloscope gain increases the measurement's vulnerability to overdrive-induced errors. At 16 bits, there is no chance of measurement integrity. Thus, measuring a 16-bit settling time requires a high-gain oscilloscope that is

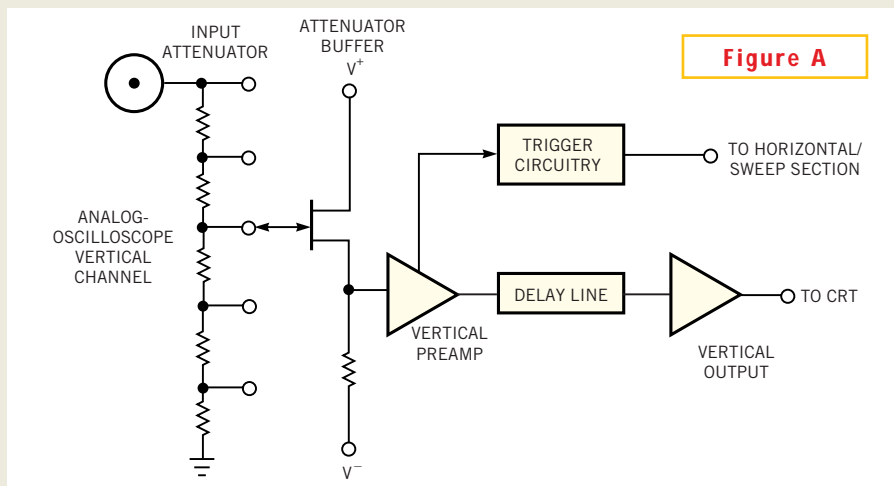
EVALUATING OSCILLOSCOPE-OVERDRIVE PERFORMANCE

The design of most of the settling-time circuits in this article attempts to provide the monitoring oscilloscope with little or no overdrive. Oscilloscope recovery from overdrive is a gray area that manufacturers almost never specify. One settling-time-measurement method requires overdriving the oscilloscope. In this case, the oscilloscope must supply an accurate waveform after the measurement circuit drives the display off screen.

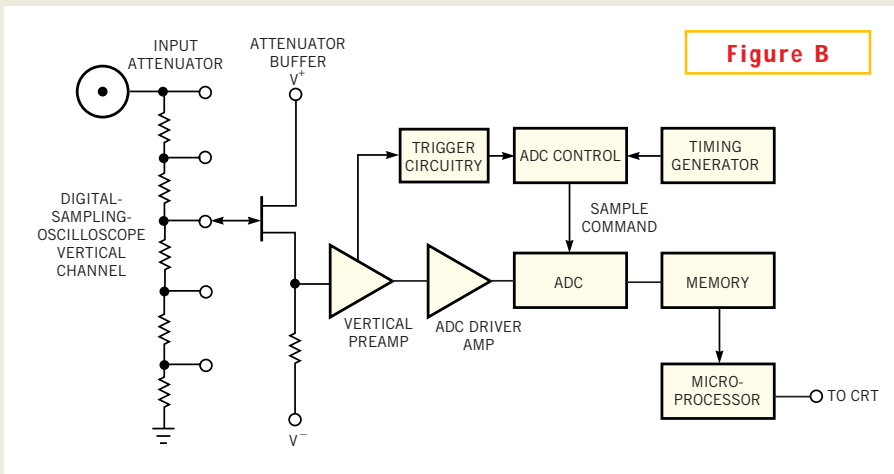
The answer to how long you must wait after an overdrive before taking the display seriously is quite complex. Factors involved in determining this duration include the degree of overdrive, its duty cycle, and its magnitude in time and amplitude.

Response to overdrive varies widely among oscilloscopes. For example, the recovery time for a 100× overload at 0.005V/div may be very different from the recovery time at 0.1V/div. The recovery characteristic may also vary with waveform shape, dc content, and repetition rate. With so many variables, you must cautiously approach measurements that involve oscilloscope overdrive.

To determine why most oscilloscopes have trouble recovering from overdrive, study the vertical paths of the three basic oscilloscopes: analog, digital, and classic sampling oscilloscopes. Analog and digital scopes are susceptible to overdrive; the classic



When you overdrive an analog oscilloscope, the attenuator buffer, preamp, and vertical output amplifier can saturate. Full recovery can take a surprisingly long time.



The linear front end of a digital sampling oscilloscope can saturate in the same way an analog scope does, causing similar overdrive-recovery problems.

somehow immune to overdrive. You can address the gain issue with an external wideband preamplifier that accurately amplifies the diode-clamped settle node. Getting around the overdrive problem is more difficult.

The only oscilloscope technology that offers inherent overdrive immunity is the classic sampling scope. Do not confuse this scope with modern-era digital sampling scopes, which have overdrive restrictions. Unfortunately, vendors no longer manufacture these classic instruments, but you can still find them on the secondary market. It is possible, however, to construct a circuit that borrows the overload advan-

tages of classic-sampling-scope technology. Additionally, you can endow the circuit with features that are particularly suitable for measuring 16-bit-DAC settling times.

A PRACTICAL SETTLING-TIME MEASUREMENT

A block diagram of a 16-bit-DAC settling-time-measurement circuit (Figure 3) shares some attributes with the circuit in Figure 2. The same pulse that controls the DAC also triggers a delayed-pulse generator, which consists of independently variable delay and pulse-generator blocks. The output of this generator determines the state of a diode-bridge switch. You adjust the delayed-pulse generator's timing so

that the switch does not close until settling is nearly complete. The circuit samples both the amplitude and the time of the incoming waveform. This scheme never subjects the oscilloscope to overdrive; no off-screen activity ever occurs. Before applying the input step to the oscilloscope, the circuit inserts a time-correction delay to compensate for the propagation delay of the settling-time-measurement path.

The diode-bridge switch is the key to the measurement. Borrowed from classic-sampling-oscilloscope circuitry, this switch connects the preamplified oscilloscope to the settle point. The diode bridge's inherent balance eliminates charge-injection-

sampling scope is the only architecture that is inherently immune to overdrive.

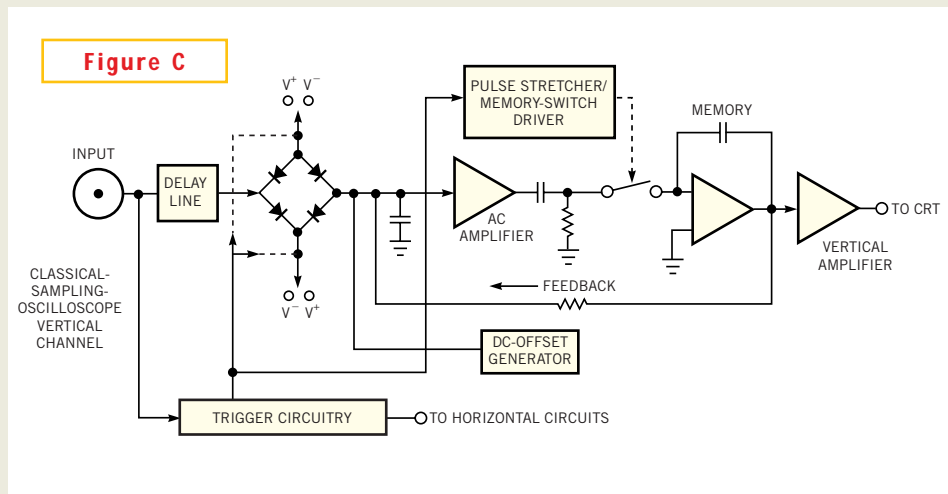
An analog oscilloscope is a real-time, continuous linear system (Figure A). The input drives an attenuator, and a wideband buffer unloads the attenuator output. The vertical preamp provides gain and drives the trigger pickoff, delay line, and vertical output amplifier. The attenuator and delay line are passive elements and require little comment.

The buffer, preamp, and vertical output amplifier are complex, linear gain blocks, each with dynamic operating-range restrictions. Additionally, inherent circuit balance, low-frequency stabilization paths, or both can set each block's operating point. Overdriving the input can cause one or more of these stages to saturate, forcing internal nodes and components to abnormal operating points and temperatures. When the overload ceases, full recovery of the electronic and thermal time constants may take a surprisingly long time.

The digital sampling oscilloscope eliminates the vertical output amplifier but has an attenuator buffer and amplifiers ahead of the A/D converter (Figure B). The digital scope is also susceptible to overdrive-recovery problems.

INSTRUMENT HAS INHERENT IMMUNITY

The classic sampling oscilloscope is unique; the nature of its operation makes it inherently immune to overload (Figure C). The classic



The classic sampling oscilloscope is inherently immune to overload because the instrument samples the input before providing any gain.

scope samples the input before taking any gain. Unlike Figure B's digital sampling scope, the input is fully passive to the sampling point. Additionally, the output feeds back to the sampling bridge, which maintains its operating point over a range of inputs. The dynamic swing available to maintain the bridge output is large and easily accommodates a range of oscilloscope inputs.

For all of these reasons, the amplifiers in the classic scope see no overload (even at 1000× overdrives) and exhibit no recovery problems. You can derive additional immunity from the instrument's relatively slow sample rate; even if you overload these amplifiers, they have plenty of time to recover between samples.

The designers of classic sampling scopes capitalized on the scope's overdrive immunity by including variable dc-offset generators to

bias the feedback loop. These generators permit you to offset a large input so that you can accurately observe small amplitude activity on top of the signal. This feature is ideal for settling-time measurements. Unfortunately, manufacturers no longer produce classic sampling oscilloscopes; if you have one, take care of it.

Don't despair if you don't have access to a classic sampling scope. Although analog and digital oscilloscopes are susceptible to overdrive, many tolerate some degree of overdrive abuse. A simple test indicates when and if overdrive deleteriously affects the oscilloscope. See Reference A for more information.

REFERENCE

A. Williams, Jim, "High-speed amplifier techniques," Application Note 47, Linear Technology Corp, 1991.

based errors in the output, making the bridge far superior to other electronic switches. Any other high-speed-switch technology contributes excessive output spikes caused by charge-based feedthrough. A FET switch is unsuitable because its gate-channel capacitance permits such feedthrough. This capacitance allows gate-drive artifacts to corrupt the oscilloscope display, inducing overload and defeating the switch's purpose.

The diode bridge's balance combines with matched, low-capacitance monolithic diodes and complementary high-speed switching to yield a cleanly switched output. The scheme also controls the temperature of the monolithic-diode bridge to provide a bridge offset error of less than 10

μV , which stabilizes the measurement baseline. Uncommitted diodes in the monolithic array implement the temperature control.

A more detailed view of the bridge circuitry reveals how the bridge diodes cancel each other's temperature coefficients (Figure 4). Unstabilized bridge drift is about $100 \mu\text{V}/^\circ\text{C}$, and the temperature control reduces residual drift to a few microvolts per degrees Celsius. To achieve temperature control, one diode acts as a sensor. Another diode, running in reverse breakdown ($V_z \approx 7\text{V}$), serves as the heater. The control amplifier, which compares the sensor diode's voltage with a voltage at the amplifier's negative terminal, drives the heater diode to stabilize the temperature of the array.

The circuit achieves dc balance by trimming the bridge's on-current for zero offset voltage between the input and output. Two ac trims are necessary: The ac-balance trim corrects for diode and layout capacitive imbalances, and the skew-compensation trim corrects timing asymmetry in the nominally complementary bridge drive. These ac trims compensate small dynamic imbalances that could result in parasitic bridge outputs.

DETAILED CIRCUIT INCLUDES SAMPLING BRIDGE

The detailed schematic of the 16-bit-DAC settling-time-measurement circuit closely follows the block diagram (Figure 5). The input pulse simultaneously switches all of the DAC bits; the pulse also routes

PRACTICAL CONSIDERATIONS FOR DAC-AMPLIFIER COMPENSATION

There are a number of practical considerations when compensating the DAC-amplifier pair to get the fastest settling time. As this article discusses, settling-time components include delay, slew, and ring times. Delay is due to the propagation time through the DAC amplifier and is a small term. The amplifier's maximum speed sets the slew time. Ring time is the time during which the amplifier recovers from slewing and ceases movement within some defined error band.

Once you choose a DAC-amplifier pair, only the ring time is readily adjustable. Because slew time is usually the dominant lag, it is tempting to select the amplifier with the

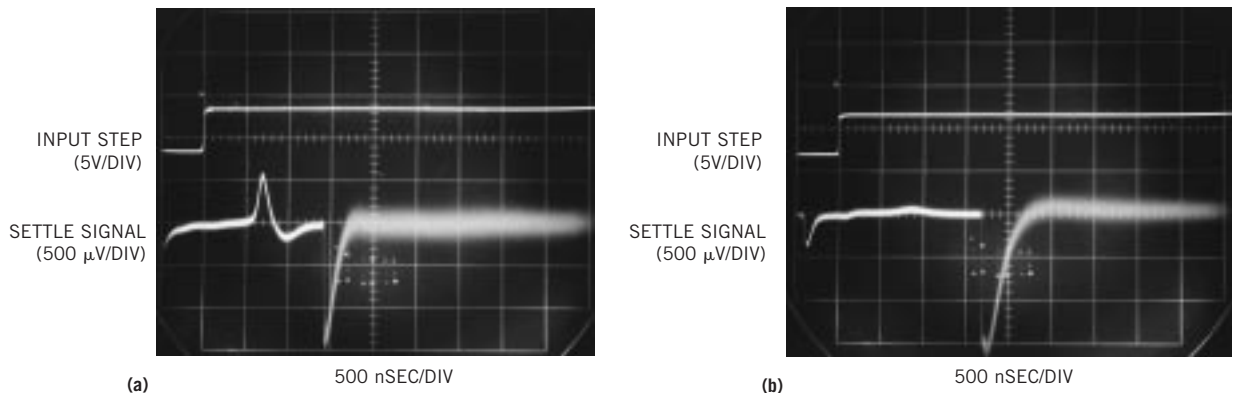
fastest available slew time to obtain the best settling. Unfortunately, fast-slewing amplifiers usually have extended ring times, negating their brute-force speed advantage. Invariably, the penalty for raw speed is prolonged ringing, which you can damp using only large compensation capacitors. This compensation works, but it results in protracted settling times.

The key to good settling times is to choose an amplifier with the right balance of slew-rate and recovery characteristics and to compensate the amplifier properly. Achieving this design goal is harder than it sounds because you can neither predict nor extrapolate an

amplifier's settling time from any combination of data-sheet specifications. You must measure the settling time in the intended configuration.

In the case of a DAC and its amplifier, a number of terms combine to influence settling time. These terms include amplifier slew rate and ac dynamics, DAC output resistance and capacitance, and the compensation capacitor. These terms interact in a complex manner, making predictions hazardous. Take notice, Spice aficionados: If you eliminate the DAC's parasitic elements and replace them with a pure resistive source, amplifier settling time is still not readily predictable. The DAC's output-

Figure A



to the oscilloscope via a delay-compensation network. This delay network, comprising CMOS inverters and an adjustable RC network, compensates the oscilloscope's input-step signal for the 12-nsec delay through the circuit's measurement path (Reference 1).

The circuit uses the 3-k Ω resistor ratio set to algebraically sum the opposing DAC amplifier, and it uses LT1236 reference currents to produce a 0V reading when the circuit settles. The LT1236 also furnishes the DAC's reference, making the measurement ratiometric. IC₁ unloads the clamped settle node and drives the sampling bridge. The additional clamp diodes at IC₁'s output prevent abnormal IC₁ outputs from damaging the diode array, which can hap-

pen because of a lost supply or supply-sequencing anomalies. (I became unfit for human companionship when I discovered this mishap. Replacing the sampling bridge was a lengthy and highly emotionally charged task that required an exhaustive breadboarding exercise. See Reference 1.) IC₃ and associated components provide temperature control for the sampling diode bridge by comparing the forward drop of the diode at pin 12 of the array with a stable potential derived from the -5V regulator. The diode at pin 14 serves as a chip heater. These pin connections provide the best temperature-control performance.

The input pulse also triggers the 74-HC123 one shot, which produces a delayed

pulse that sets the diode bridge on time. The 20-k Ω potentiometer sets the delay, and the 5-k Ω potentiometer sets the pulse width. If you appropriately set the delay, the oscilloscope does not see any input until settling is nearly complete, eliminating overdrive to the scope. You need to adjust the sample-window width so that you can observe all remaining settling activity. In this way, the oscilloscope's output is reliable, and you can observe meaningful data. Q₁ through Q₄ shift the level of the one shot's output to provide the bridge with a complementary switching drive. The switching transistors (Q₁ and Q₂) are UHF types; they permit true differential bridge switching with less than 1 nsec of time skew.

impedance terms make this difficult problem even more messy.

The only way to deal with these problems is to use the feedback compensation capacitor, C_F. C_F rolls off amplifier gain at the frequency that permits the best dynamic response. Normally, the DAC's current output unloads directly into the amplifier's summing junction, placing the DAC's parasitic capacitance between ground and the amplifier's input. The capacitance introduces feedback phase shift at high frequencies, forcing the amplifier to "hunt" and ring around the final value before settling. Different DACs have different output-capacitance values. CMOS DACs have the highest output capacitance, typically 100 pF. This value varies with code.

You can achieve the best settling results by

selecting the compensation capacitor to functionally compensate for all of the mentioned parasitics. **Figure Aa** shows results for an optimally selected feedback capacitor. The amplifier comes cleanly out of slew and settles quickly.

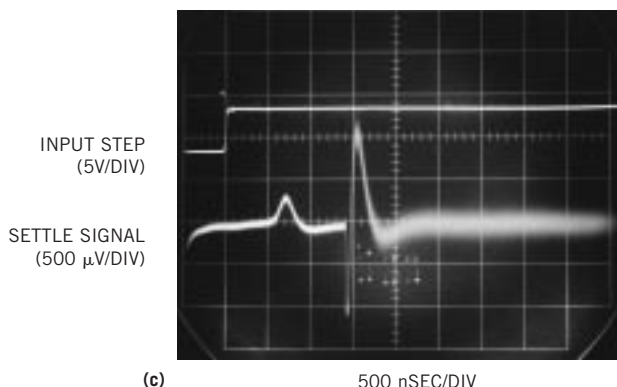
In **Figure Ab**, the feedback capacitor is too large. Settling is smooth, although overdamped, and a 600-nsec penalty results.

Figure Ac's feedback capacitor is too small, causing a somewhat underdamped response and resulting in excessive ring-time excursions. In both cases, settling time increases from 1.7 to 2.3 μ sec.

When you individually trim the feedback capacitor for optimal response, the DAC, amplifier, and compensation-capacitor tolerances are irrelevant. If you don't use individ-

ual trimming, you must consider these tolerances when determining the feedback capacitor's production value. DAC capacitance and resistance, as well as the feedback capacitor's value, affect the ring time. The relationship is nonlinear, although some guidelines are possible. The DAC-impedance terms can vary by $\pm 50\%$, and the feedback capacitor is typically a $\pm 5\%$ component. Additionally, the data sheet states that amplifier slew rate has a significant tolerance. To obtain a production feedback-capacitor value, determine the optimum value by individually trimming components on the production-board layout. (Board-layout parasitic capacitance counts, too.) Then, factor in the worst-case percentage values for DAC-impedance terms, slew rate, and feedback-capacitor tolerance. Add these values to the trimmed capacitor's measured value to obtain the production value. This budgeting is perhaps unduly pessimistic, but it will keep you out of trouble. (Summing the rms error may be a defensible compromise, but this method's potential problems become clear when you are sitting in an airliner that is landing in a snow-storm.)

An optimal value of C_F compensates for all DAC parasitics and results in the fastest settling time of 1.7 μ sec (a). Increasing the capacitor's value produces an overdamped response with no ringing, but settling time increases to 2.3 μ sec (b). An undersized capacitor produces an underdamped response with additional ringing that also results in a longer settling time of 2.3 μ sec (c).



The residue amplifier (IC_2) monitors the bridge's output, provides gain, and drives the oscilloscope. **Figure 6** shows circuit waveforms. When the sample gate goes low, the bridge switches cleanly, and you can easily observe the last 1.5 mV of slew. Ring time is also clearly visible, and the amplifier settles nicely to its final value. When the sample gate goes high, the bridge switches

off, with only 600 μ V of feedthrough. The 100- μ V peak before bridge switching (at ≈ 3.5 vertical divisions) is evidence of feedthrough from IC_1 's output, but the circuit controls this feedthrough to keep all activity on screen. No off-screen activity occurs at any time; the circuit never subjects the oscilloscope to overdrive.

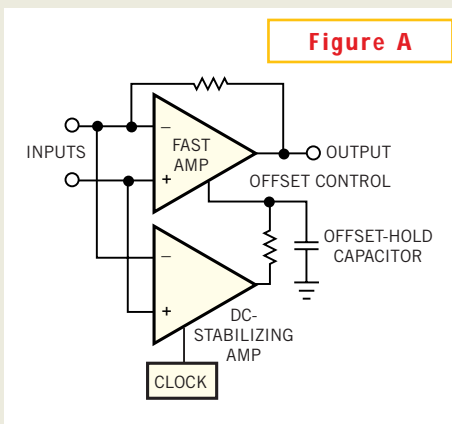
The circuit requires trimming to achieve

this level of performance. Grounding Q_5 's base before applying power sets the bridge's temperature-control point. Next, apply power and measure IC_3 's positive input with respect to the -5 V rail. Select the resistor at IC_3 's negative input, which is nominally 1.5 k Ω , for a voltage at IC_3 's negative input that is 57 mV less than the positive input's value. As before, adjust IC_3 's nega-

MEASURING THE SETTLING TIME OF CHOPPER-STABILIZED AMPLIFIERS

Determining the settling time of chopper-stabilized amplifiers is a special case and requires some understanding of how these amplifiers work. **Figure A** is a simplified block diagram of the LTC1150 CMOS chopper-stabilized amplifier, which actually includes two amplifiers. The "fast amp" processes input signals directly to the output. This amplifier is relatively quick, but it has poor dc-offset characteristics. A second, clocked amplifier periodically samples the offset of the fast channel and maintains an offset-hold capacitor at whatever value is necessary to correct the fast amplifier's offset errors. The circuit clocks the dc-stabilizing amplifier so that it operates (internally) as an ac amplifier, eliminating its dc terms as an error source. The clock chops the stabilizing amplifier at about 500 Hz, providing the hold-capacitor-offset control with updates every 2 msec.

The settling time of this composite amplifier is a function of the response of the fast and stabilizing paths. **Figure Ba** shows short-term



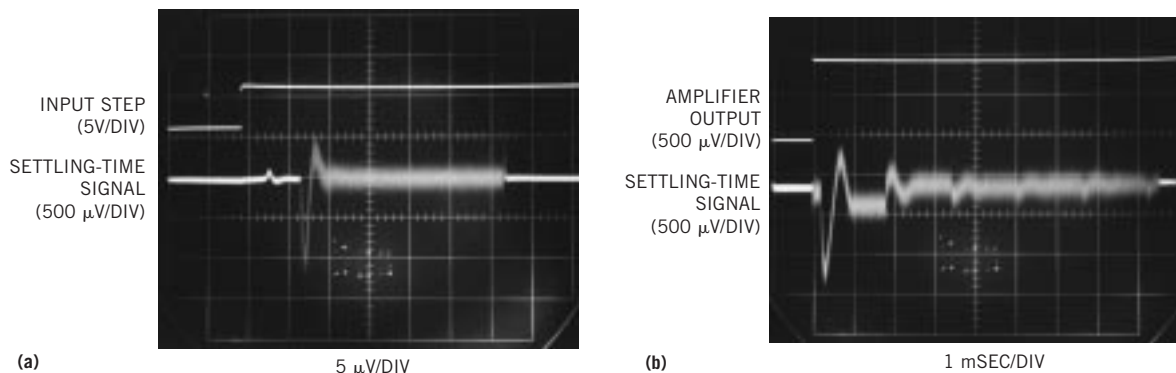
An LTC1150 CMOS chopper-stabilized amplifier comprises a fast amp, which processes signals directly to the output, and a dc-stabilizing amp, which periodically samples the offset of the fast amp and maintains its output-hold capacitor at a value that minimizes offset errors.

huge error 200 μ sec later, when the internal clock applies an offset correction. Successive clock cycles progressively chop the error into the noise, but a complete recovery takes 7 msec.

The error occurs because the amplifier samples its offset when its input signal is well outside its bandpass. This set of events causes the stabilizing amplifier to acquire erroneous offset information. When the amplifier applies the "correction," a huge output error results. Admittedly, this error is a worst-case scenario; it can happen only if the DAC's slew-time interval coincides with the amplifier's internal clock cycle—but it can happen.

settling of the amplifier. Damping is reasonable, and the 10- μ sec settling time and profile appear typical. **Figure Bb** reveals an unpleasant surprise. If the DAC's slew-time interval coincides with the amplifier's sampling cycle, serious error results. In **Figure Bb**, the horizontal scale is slow. Initially, the amplifier quickly settles (settling is visible in the second vertical-division region), but it generates a

Figure B



The short-term settling profile of the chopper-stabilized amplifier seems typical at approximately 10 μ sec (a). Unfortunately, slowing the horizontal sweep reveals a monstrous tailing error, which occurs when the amplifier's clocked operation coincides with DAC slewing (b).

tive input with respect to $-5V$. Remove ground from Q_5 's base, and the circuit will control the sampling bridge to about $55^\circ C$ according to the following equation:

$$25\text{ C (ROOM)} + \frac{57\text{ mV}}{1.9\text{ mV/ C (DIODE DROP)}} = 25\text{ C} + 30\text{ C (RISE)} = 55\text{ C.}$$

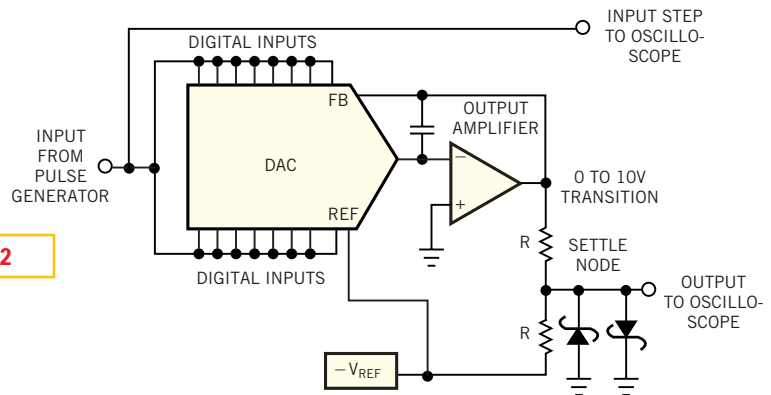
You set the dc and ac bridge trims—baseline zero, ac balance, and skew compensation—when the temperature control is functional. To make these adjustments, disable the DAC and its amplifier by disconnecting the input pulse from the DAC, setting all DAC inputs low, and shorting the settle node directly to the ground plane. When the switching-related activity is on-screen and the offset error reduces to an unreadable level, the circuit is ready to use. You can remove ground from the settle node and restore the input-pulse connection to the DAC.

Beware that without proper trimming, ac and dc errors are present at the output of IC_2 's residue amplifier. The sample gate's transitions cause large, off-screen residue-amplifier swings, and the amplifier output shows significant dc-offset error during the sampling interval. Adjusting the ac-balance and skew-compensation potentiometers minimizes the switching-induced transients.

SET SAMPLING WINDOW AND COMPENSATION

Figure 7 underscores the importance of proper sampling-window positioning in time. In Figure 7a, the sample gate's delay

Figure 2



A popular summing scheme for DAC-settling-time measurements provides misleading results because a 16-bit measurement causes greater than $200\times$ oscilloscope overdrive, and the scope displays meaningless information.

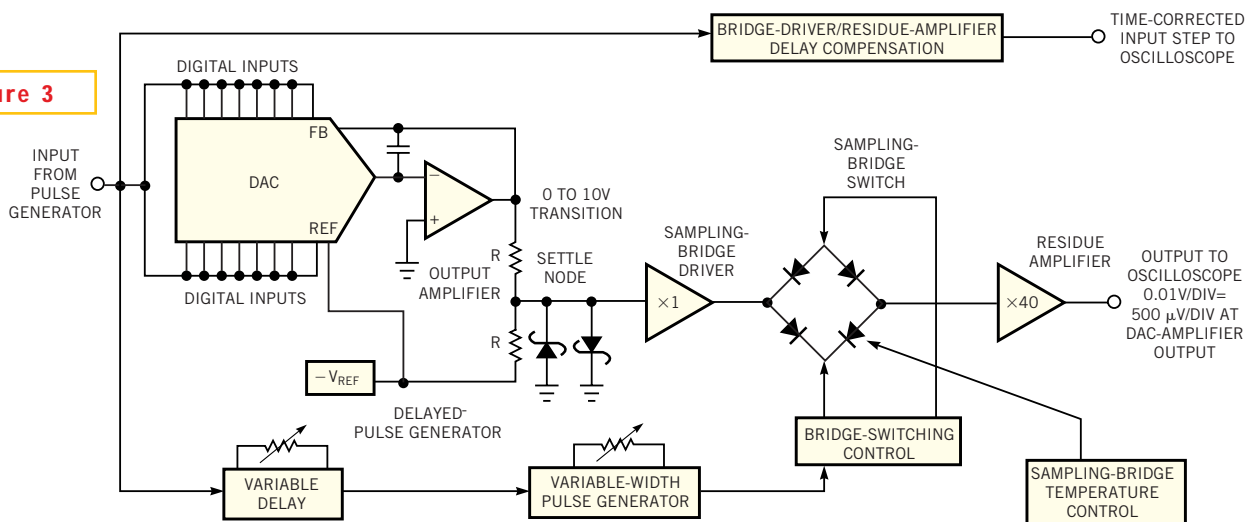
initiates the sample window too early, and the residue amplifier's output overdrives the oscilloscope when sampling commences. Figure 7b displays optimal conditions, with all amplifier residue well within the screen boundaries.

In general, it is good practice to "walk" the sampling window until the last millivolt or so of the amplifier's slew time so that you can observe the onset of ring time. The sampling-based approach provides this capability, which is a powerful measurement tool. Additionally, remember that slower amplifiers may require extended delay times, extended sampling-window times, or both. These extended times may necessitate larger capacitor values in the 74H123 one-shot timing networks.

The DAC-amplifier pair requires fre-

quency compensation to achieve the best possible settling time. The DAC has appreciable output capacitance, which complicates amplifier response and makes careful compensation-capacitor selection even more important (see sidebar "Practical considerations for DAC-amplifier compensation"). Light compensation permits very fast slew times but causes excessive ringing amplitude over a protracted time, which increases the total settling time. Severe ringing can feed through during a portion of the sample-gate off period, although no overdrive results. A large-value compensation capacitor eliminates all ringing but slows the amplifier and further increases settling time. A carefully chosen compensation capacitor results in tightly controlled damping.

Figure 3



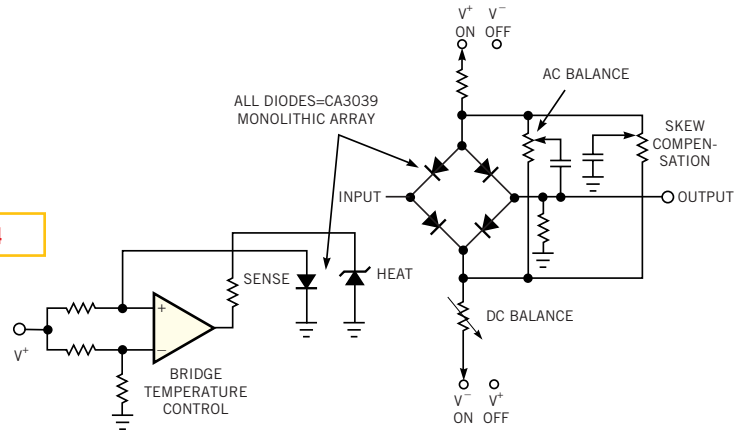
A diode-bridge-switch scheme minimizes switching feedthrough, which prevents the residue amplifier from overdriving the oscilloscope. Temperature control maintains a $10\text{-}\mu V$ switch-offset baseline.

ALTERNATIVE METHODS VERIFY RESULTS

Based on the above results, the sampling-based settling-time circuit appears to be a useful measurement option, but how can you be sure? A good way to verify **Figure 5's** method is to make the same measurement using alternative methods and see if you get the same results.

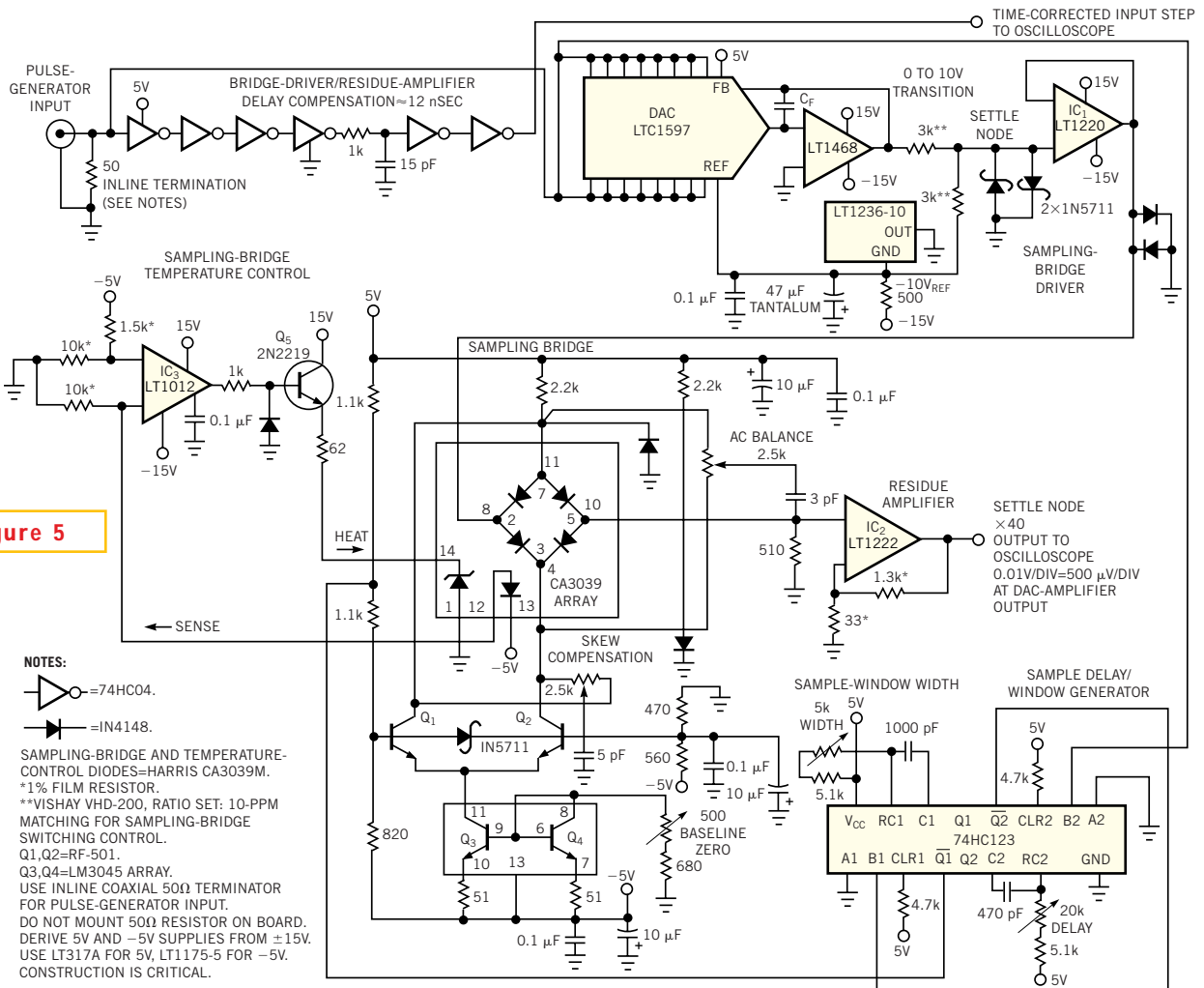
Recall from **Figure 2** that the Schottky-diode-bounded settle node forces a 400-mV overdrive to the oscilloscope, rendering all measurements useless. Now, consider the result if the diodes return to bias voltages that are slightly lower than the diode drops. Theoretically, this setup has the same effect as ground-referred diodes with an inherently lower forward drop, which greatly reduces oscilloscope overdrive. In practice, diode V-I characteristics

Figure 4



A more detailed schematic of the diode-bridge switch includes adjustments for ac balance, dc balance, and switch-drive timing skew. Two uncommitted diodes in the diode array provide the sense and heat temperature controls.

Figure 5



NOTES:

- ▷ = 74HC04.
- ▷ = 1N4148.
- SAMPLING-BRIDGE AND TEMPERATURE-CONTROL DIODES=HARRIS CA3039M.
- *1% FILM RESISTOR.
- **VISHAY VHD-200, RATIO SET: 10-PPM MATCHING FOR SAMPLING-BRIDGE SWITCHING CONTROL.
- Q1,Q2=RF-501.
- Q3,Q4=LM3045 ARRAY.
- USE INLINE COAXIAL 50Ω TERMINATOR FOR PULSE-GENERATOR INPUT.
- DO NOT MOUNT 50Ω RESISTOR ON BOARD.
- DERIVE 5V AND -5V SUPPLIES FROM ±15V.
- USE LT317A FOR 5V, LT1175-5 FOR -5V.
- CONSTRUCTION IS CRITICAL.

A detailed schematic of the DAC-setting-time-measurement circuit includes the DAC and its output amplifier, the temperature-controlled diode-bridge switch, time-correction circuitry for the input step to the oscilloscope, and a delayed-pulse generator for proper positioning of the sample window.

and temperature effects limit achievable performance to uninteresting levels. Clamping reduction is minimal, and diode forward leakage, which occurs when the settle node reaches zero, causes signal amplitude errors. Although this approach is impractical, it hints at a more useful method.

METHOD I: BOOTSTRAPPED CLAMP

One approach returns the diodes to amplifier-generated voltages bootstrapped from the settle node's input signal (Figure 8). This method maintains the diode bias at the optimum point with respect to the settle-node signal. During DAC-amplifier slew, the settle-node signal is large, and the amplifiers supply a resultant large bias to the diodes, forcing the desired small clamp voltage. When the DAC-amplifier comes out of slew, the settle-node signal nearly approaches zero, the clamp amplifiers supply almost no diode bias, and the oscilloscope monitors the uncorrupted settle-node output. Adjustable amplifier gains permit optimal setting of positive and negative bound limits. This scheme offers the possibility of minimizing oscilloscope overdrive and preserving signal-path integrity.

The circuit in Figure 9 adapts the bootstrapped clamp to Figure 6's settling-time test circuit. The clamp circuit, comprising IC₃ and IC₄, is nearly identical to Figure 8's circuit. The settle node feeds the residue amplifier (IC₁ and IC₂), which drives the boot-

strapped clamp. IC₁ and IC₂ supply a non-saturating gain of 80 to the clamp, which permits a 500- μ V/div oscilloscope scale factor with respect to the DAC-amplifier output. As before, the circuit time corrects the input pulse for signal-path delays. Additionally, FET probes at the outputs ensure overall delay matching. The bootstrapped clamp's output impedance mandates a FET probe. A second FET probe can monitor the input step but only to maintain channel-delay matching.

METHOD II: SAMPLING OSCILLOSCOPE

As previously discussed, classic sampling oscilloscopes are inherently immune to overdrive, so why not use this feature and attempt to measure settling time using a simple diode clamp? The circuit in Figure 10 is identical to that in Figure 9, except that a simple diode clamp replaces the bootstrapped clamp. These conditions heavily overdrive the sampling scope—a Tektronix (www.tek.com) type 661 with

4S1 vertical and 5T3 timing plug-ins—which is ostensibly immune to the overdrive insult.

METHOD III—DIFFERENTIAL AMPLIFIER

In theory, a differential amplifier that has one input biased at the expected settled voltage can measure settling time to 16-bit resolution. In practice, this measurement is extraordinarily demanding for a differential amplifier. The amplifier's overload-recovery characteristics must be pristine. In fact, no commercially produced differential-amplifier or -oscilloscope plug-in meets this requirement. However, a recently introduced instrument, the differential amplifier type 1855 from Preamble Instruments (www.preamble.com), which is not fully specified at these levels, appears to have superb overload-recovery performance (Figure 11). An internal adjustable reference biases the amplifier's negative input to the expected settled voltage. The differential amplifier's clamped output operates at a gain of 10 and drives IC₁ and IC₂. Together, IC₁ and IC₂ produce a bounded, non-saturating gain of 40. This circuit cannot overdrive the monitoring oscilloscope, which operates at 0.2V/div (500 μ V/div at the DAC amplifier).

SUMMARIZE THE RESULTS

The simplest way to summarize the results of these four measurement techniques is by visual comparison. Figure 12 displays the settling times of all four circuits. If all four ap-

Figure 6

INPUT PULSE
(10V/DIV)
DAC-AMPLIFIER
OUTPUT
(10V/DIV)
SAMPLE GATE
(10V/DIV)
SETTLING-TIME
OUTPUT
(500 μ V/DIV)

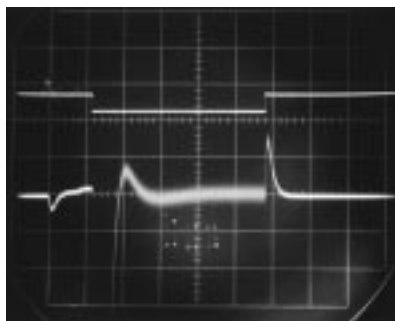


1 μ SEC/DIV

With proper trimming and proper positioning of the sample gate's window, the settling-time measurement is 1.7 μ sec.

Figure 7

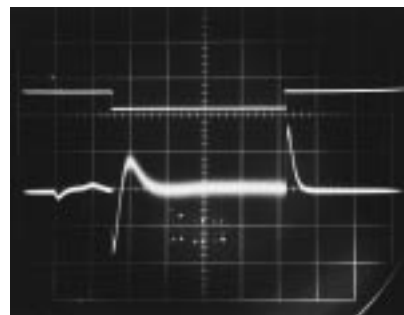
SAMPLE WINDOW
(10V/DIV)
RESIDUE-AMPLIFIER
OUTPUT
(500 μ V/DIV)



(a)

1 μ SEC/DIV

SAMPLE WINDOW
(10V/DIV)
RESIDUE-AMPLIFIER
OUTPUT
(500 μ V/DIV)



(b)

1 μ SEC/DIV

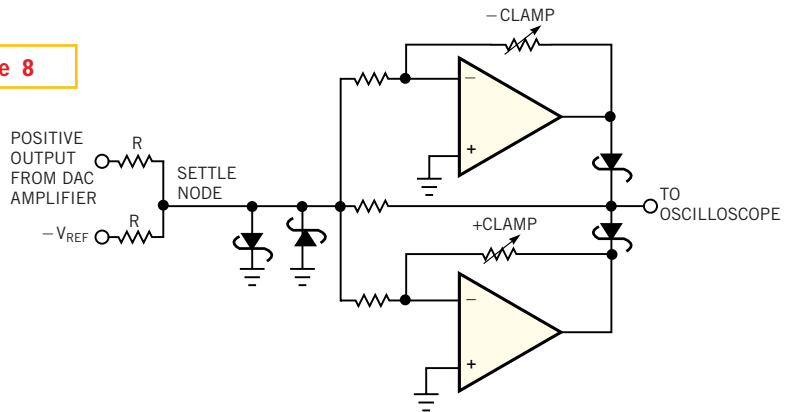
Properly positioning the sampling window in time is critical. Inadequate sample-gate delay overdrives the oscilloscope and results in off-screen activity (a). The optimal delay time positions the sampling window so that all output settling information is well within the screen's boundaries (b).

designfeature *Measuring 16-bit-DAC settling time*

proaches represent good measurement techniques and if you properly construct each circuit, the results should be identical. If the results are identical, they have a high probability of being valid. Remember that the construction details are critical.

Examination of the four scope photos in **Figure 12** shows identical 1.7- μ sec settling times and settling-waveform signatures. The shape of the settling waveform is identical in all four photos. In each photo, the top trace is the time-corrected input step, and the bottom trace is the settle signal. In the bootstrapped-clamp circuit, the oscilloscope undergoes about a 2.5 \times overdrive, although the settling signal appears undistorted (**Figure 12b**). Despite a brutal overdrive of the classic sampling scope, the scope appears to respond cleanly, giving a plausible settle-signal presentation (**Figure 12c**). For the differential-amplifier circuit, the settle signal comes smoothly out of

Figure 8



A bootstrapped clamp biases the diodes from the settle-node input signal to minimize the effects of V-I characteristics and temperature.

bound, entering the amplified linear region between the third and fourth vertical divisions (**Figure 12d**). The settling signature appears reasonable, and complete settling occurs just beyond the fourth vertical di-

vision. This kind of agreement makes the measured results highly credible. It also provides you with the confidence to characterize a variety of amplifiers.

When discussing DAC settling time, you

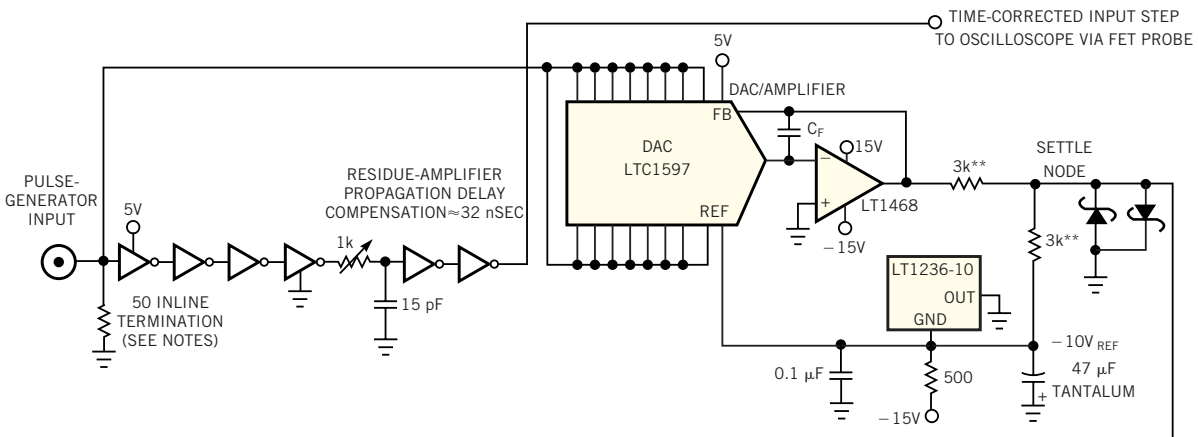
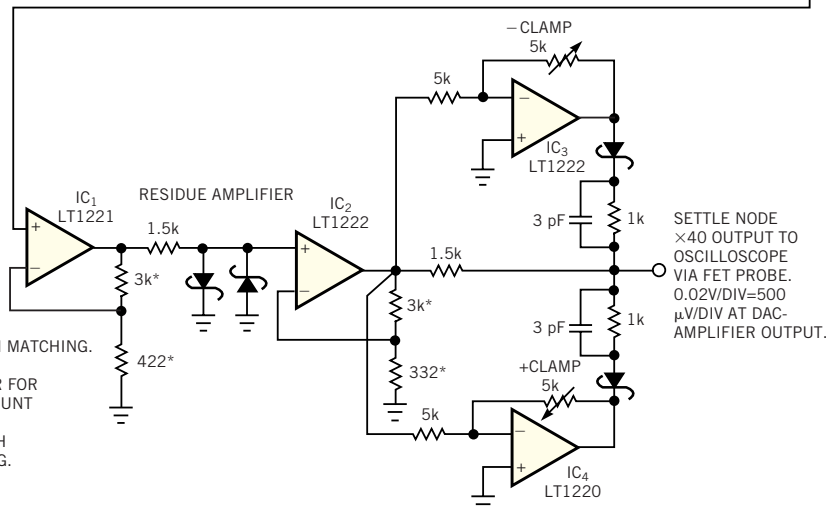


Figure 9

NOTES:

— = 74HC04.
 = IN4148.

*1% FILM RESISTOR.
 **VISHAY VHD-200, RATIO SET: 10-PPM MATCHING.
 BYPASS ALL ICs.
 USE INLINE COAXIAL 50 Ω TERMINATOR FOR PULSE-GENERATOR INPUT. DO NOT MOUNT 50 Ω RESISTOR ON BOARD.
 USE SAME TYPE FET PROBES FOR BOTH OUTPUTS TO ENSURE DELAY MATCHING.
 CONSTRUCTION IS CRITICAL.



SETTLE NODE
 $\times 40$ OUTPUT TO
 OSCILLOSCOPE
 VIA FET PROBE.
 0.02V/DIV=500
 μ V/DIV AT DAC-
 AMPLIFIER OUTPUT.

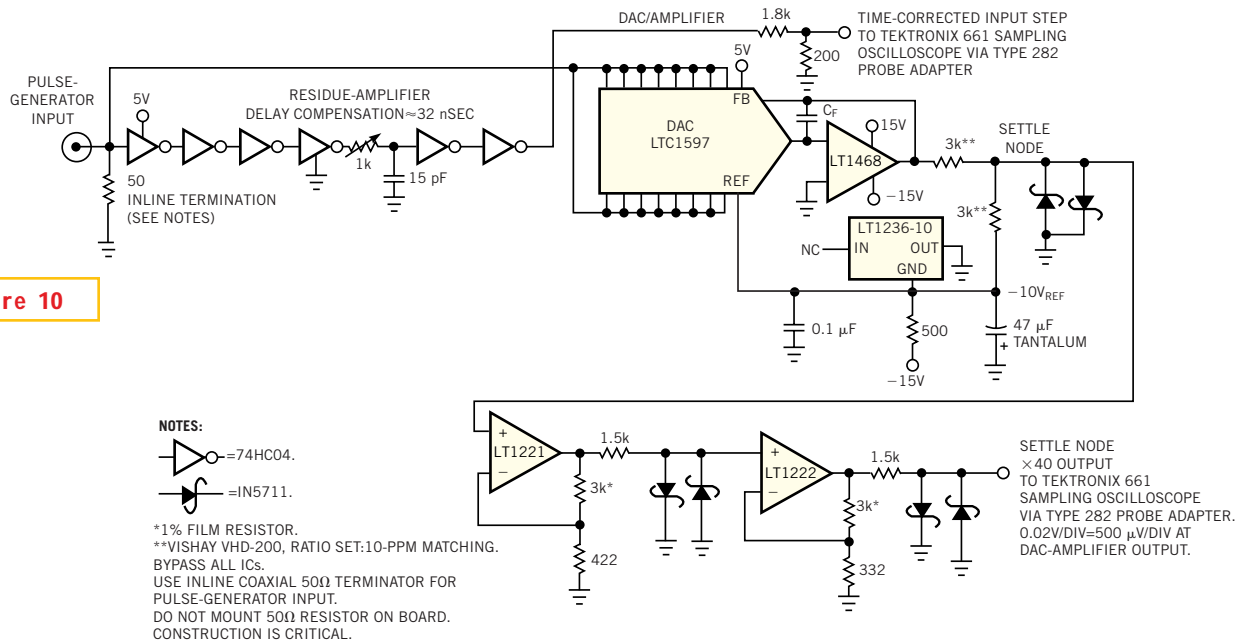
A bootstrapped-clamp-based settling-time-measurement circuit results in a substantially lower oscilloscope overdrive than you get with the conventional diode clamp, but the oscilloscope must still tolerate $\approx 2.5\times$ screen overdrive.

designfeature *Measuring 16-bit-DAC settling time*

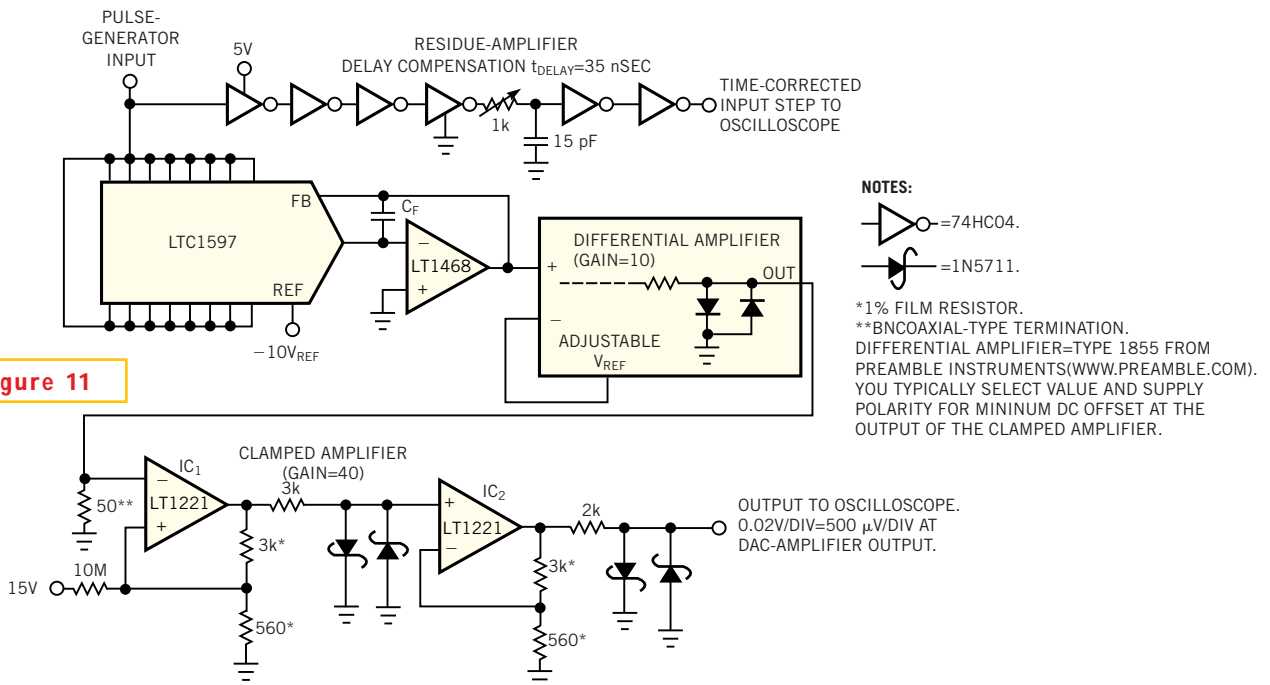
cannot isolate the DAC from its output amplifier; the DAC-amplifier combination is crucial to obtaining the performance you desire. However, beware of oversimplifying this complex topic. A suitable amplifier for

your application may not be accurate to 16 bits over temperature or, in some cases, even at 25°C. Many applications, such as ac signal processing, servo loops, and waveform generation, are insensitive to dc-off-

set error. Therefore, amplifiers that are not accurate to 16 bits may still be worthy candidates. Applications requiring dc accuracy to 16 bits (10V full-scale) must keep input errors at less than 15 nA and 152 μV

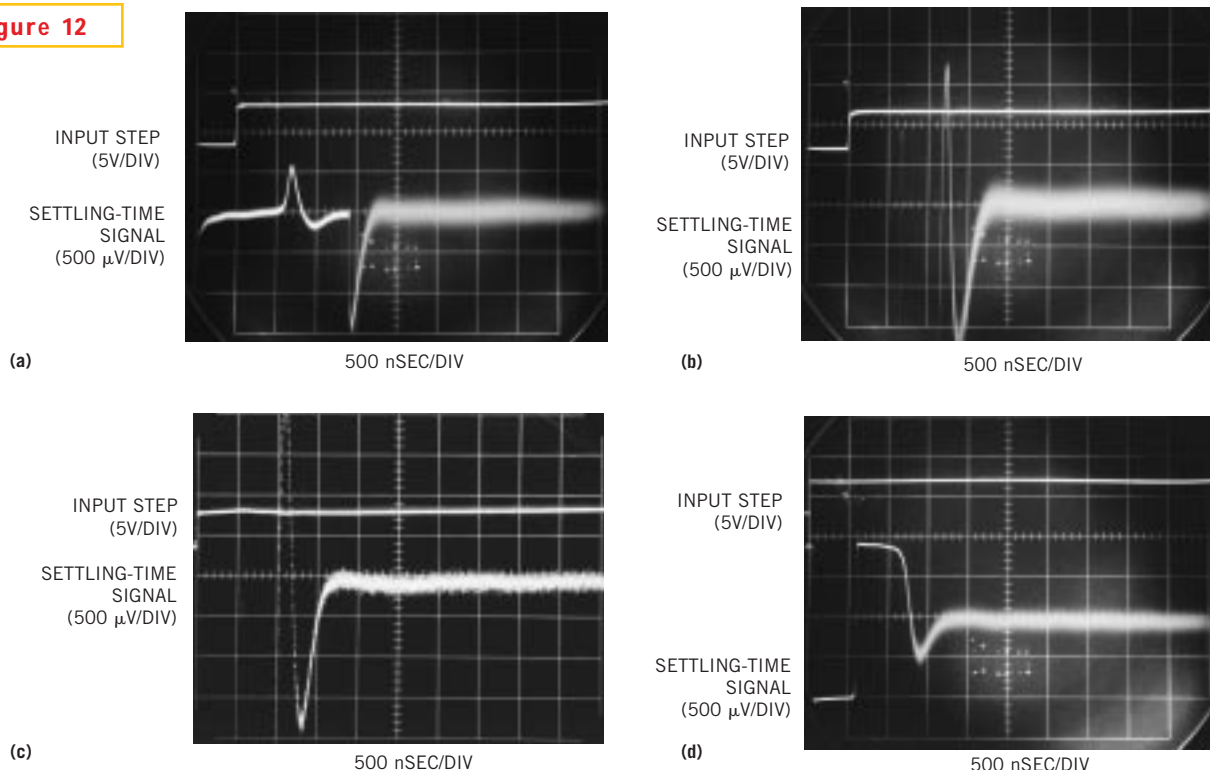


A classic sampling oscilloscope's inherent overload immunity allows you to use a simple diode clamp in place of a bootstrapped clamp.



A differential amplifier with excellent input-overload recovery allows 16-bit settling-time measurements without overdriving the oscilloscope.

Figure 12



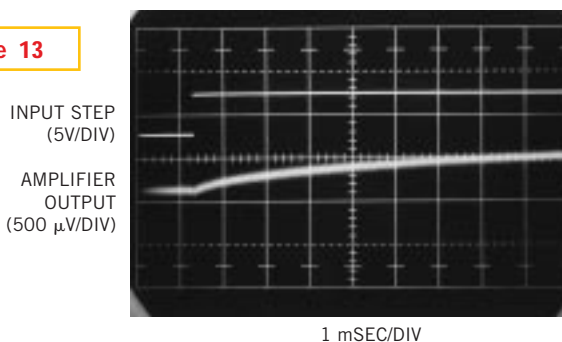
Settling-time-measurement results of all four techniques—the original diode-bridge circuit (a), the bootstrapped-clamp method (b), the simple diode clamp with a classic sampling oscilloscope (c), and the differential-amplifier approach (d)—show identical 1.7-μsec settling times and identical settling-waveform signatures.

to maintain performance. Amplifiers with 16-bit accuracy fall into two categories: amplifiers with absolute dc conformance at room temperature and amplifiers with absolute dc conformance over temperature.

All amplifiers have an inherent accuracy-versus-speed trade-off. Some very accurate amplifiers are relatively slow. Ask yourself two important questions: Do you really need 16 bits over temperature and how fast do you need to go? The circuit in **Figure 6** combines the LTC1597 DAC and the LT1468 amplifier for a blend of 16-bit accuracy and a 1.7-μsec settling time.

A final category of settling-time error is thermally based. Some poorly designed amplifiers exhibit a substantial “thermal tail” after responding to an input step. This phenomenon, due to die heating, can cause

Figure 13



A poorly designed amplifier can exhibit a “thermal tail,” which is drift due to die heating, even after it appears that settling has occurred. In this case, loading the amplifier causes a thermal-tail error of 400 μV, or greater than 2.5 LSB.

the output to wander outside desired limits long after the output appears settled. After checking settling at high speed, it is always a good idea to slow the oscilloscope sweep and look for thermal tails (**Figure 13**). The loaded amplifier slowly drifts 400 μV after apparent settling (note horizontal-sweep speed). Often, loading the amplifier’s output accentuates the thermal tail’s effect.

Reference

1. Williams, Jim, “Component and measurement advances ensure 16-bit DAC settling time,” Application Note 74, Linear Technology Corp, 1998.

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Author’s biography

Jim Williams is a staff scientist at Linear Technology Corp (Milpitas, CA, www.linear-tech.com), where

he specializes in analog-circuit and instrumentation design. He has served in similar capacities at National Semiconductor, Arthur D Little, and the Instrumentation Laboratory at the Massachusetts Institute of Technology (Cambridge, MA). A former student at Wayne State University (Detroit), Williams enjoys art, collecting antique scientific instruments, and restoring old Tektronix oscilloscopes.