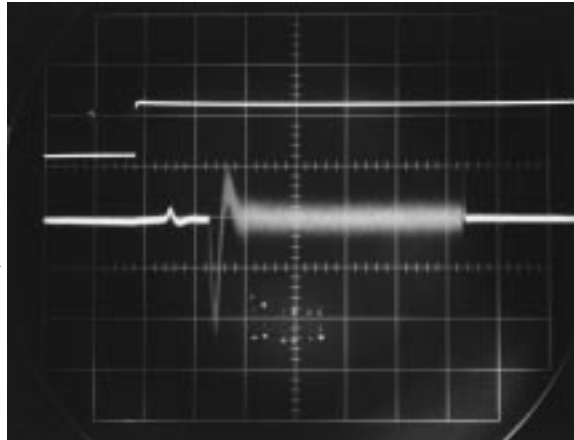


## Figure B

a)

INPUT STEP  
(5V/DIV)

SETTLING-TIME SIGNAL  
(500 $\mu$ V/DIV)

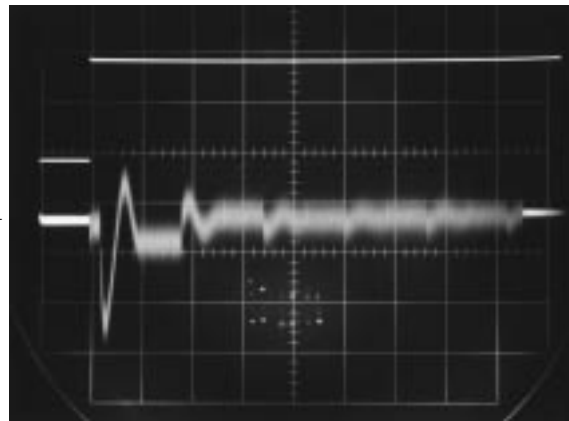


5  $\mu$ V/DIV

b)

AMPLIFIER-OUTPUT  
(500 $\mu$ V/DIV)

SETTLING-TIME SIGNAL  
(500 $\mu$ V/DIV)



1 mSEC/DIV

**The short-term settling profile of the chopper-stabilized amplifier seems typical at approximately 10  $\mu$ sec (a). Unfortunately, slowing the horizontal sweep reveals a monstrous tailing error, which occurs when the amplifier's clocked operation coincides with DAC slewing (b).**