



Power-on reset

Many digital-design teams assign the design of the power-on-reset circuit to their youngest, least experienced engineer. This assignment is a mistake. Let me explain why.

In their first power-on-reset experience, most new engineers gravitate toward a circuit like the one in

Figure 1. This circuit works beautifully in simulation, assuming that the V_{CC} voltage rises quickly and monotonically to its maximum value and stays there. Under those conditions, you can choose an RC time constant large enough to guarantee that the Schmitt-trigger gate holds \sim RESET low (active) for any specified time after V_{CC} stabilizes. After the RC timeout, \sim RESET goes high (inactive), commencing normal operations.

Circuits like this are in widespread use. At one time in my career, a distributor of telecommunications equipment hired me to evaluate 85 brands of small-office telephone products. Phone equipment is supposed to be extremely reliable. I therefore decided to test each product to determine its susceptibility to various external influences, including power quality. My power-quality tester consisted of a big, adjustable Variac autotransformer for simulating brownout conditions and a relay circuit that could interrupt power for 100 to 1000 msec.

I chose the power-interruption test because it mimics the way power outages most often happen in the real world. Power outages often begin when a foreign object, such as a tree branch, squirrel, or bird, comes into contact with the power lines. This event draws a large amount of cur-

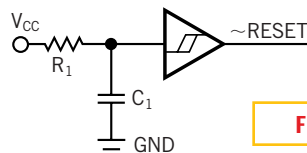


Figure 1

This power-on-reset circuit is simple yet flawed.

rent, which shorts out the power voltage while creating one crispy-fried squirrel or bird. After a couple of hundred milliseconds, the local neighborhood circuit breaker that feeds the shorted area blows open. Once that circuit breaker takes the faulty neighborhood offline, everybody else's power recovers. If you live outside the faulty neighborhood (statistically likely), you see only a momentary glitch and then a quick recovery of the power voltage. It happens all the time.

Power interruptions drive power-on-reset circuits crazy. Consider what a power dropout does to the circuit in **Figure 1**. Imagine that the RC time constant in

this **figure** is 1 sec. Let V_{CC} come up and stabilize at full voltage for perhaps 10 sec. Next, apply an ac power interruption just long enough to drop V_{CC} to 0V for about 100 msec. If a processor is involved, the dropout is long enough to make scrambled eggs of the processor's internal state machines but not long enough to discharge the RC circuit. If the RC circuit doesn't discharge, \sim RESET doesn't activate, and the processor spins out of control, powered on, but lost in space.

The effects of power-on-reset debacles in a big system can be hilarious. In poorly designed phone equipment, the dropout test causes all kinds of failures, including crossed calls, bleeping phones, and smoking power supplies. The failed systems usually don't wake up again until you completely remove power, wait a few seconds, and then restore it in the ordinary way. For most systems, the simple RC-based power-on-reset circuit is completely inadequate.

A good power-on-reset circuit must activate when power is currently good and has been good for some time and must completely and quickly deactivate upon any indication of poor power quality. That situation is what you find in equipment that passes the dropout test.

A good power-on-reset designer understands ac power systems, dc power systems, microprocessors, and some analog design. This person is unlikely to be a young, inexperienced engineer. If someone asks you to design a power-on-reset circuit, don't take the assignment lightly. Design a good circuit and test it well.

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