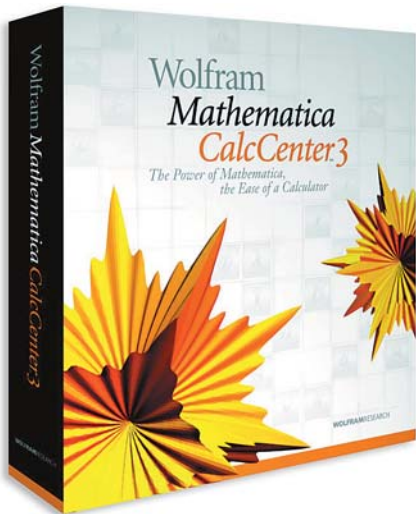


pulse

INNOVATIONS & INNOVATORS

Easy-to-use math software promises Mathematica's speed and accuracy



According to the vendor, Mathematica CalcCenter 3 combines the speed and accuracy of its progenitor, Mathematica, with extreme user friendliness and complete file compatibility with the established package.

Wolfram Research says that its new Mathematica CalcCenter 3 delivers the speed and accuracy of the company's flagship Mathematica package in a version that new users can get up and running in as little as 10 minutes. The target audience for the new package includes users who believe that their computational requirements have outgrown the capabilities of Excel, Mathcad, or Maple. CalcCenter 3 not only brings new speed and accuracy to high-powered math software, says a company spokesperson, but also is fully compatible with Mathematica itself. You can move notebook files back and forth between Mathematica and CalcCenter 3 as often as you wish. The underlying algorithms and technology are identical, and the speed with which CalcCenter 3 obtains results is just as great as that of its more powerful sibling.

Wolfram also says that, by leveraging the development of CalcCenter 3 on the established Mathematica, it reduced development costs and thereby more attractively priced the easy-to-use package than it could have had it built the new package from the ground up. Mathematica CalcCenter 3 carries a list price of \$595 in the United States and Canada. The academic list price is \$195, and a student version costs \$99.95.—**by Dan Strassberg**

► **Wolfram Research Inc.**, www.wolfram.com.

Serial-pulse-data generator produces 7-GHz patterns

Agilent Technologies has announced a high-speed, serial-pulse-data generator with stimulus capability to 7 GHz. According to the company, the 81141A is the first pulse generator to achieve such speeds. By providing precision low-jitter signals and offering full control of data streams for stress tests, the \$88,000 instrument enables computer- and semiconductor-test engineers to accurately characterize components for the next-generation, high-speed serial buses. The unit's 1-GHz linear-delay modulation enables fast and precise jitter-tolerance and jitter-transfer measurements.



The 81141A provides serial pulse trains at rates to 7 GHz for physical-layer testing of ultrahigh-speed serial buses.

"Combining multiple data formats, such as RZ [return to zero], R1 [return to one], and NRZ [non-return to zero], with sequencing, trigger capability, and fast frequency change, is unique in the market and is critical for the next-generation high-speed-technology wave," says Siegfried Gross, vice president and general manager of Agilent's Digital Verification Solutions Division. "High-speed design starts with the physical layer and its signal integrity."—**by Dan Strassberg**

► **Agilent Technologies**, www.agilent.com/find/7g_pulse.

Bluetooth chip targets stereo headsets

Broadcom has rolled out its first Bluetooth chip for wireless-stereo headsets. The single-chip BCM-2037 includes Bluetooth EDR (enhanced-data-rate) functions for enhanced audio quality and extended battery life. Broadcom officials state that this chip is the first Bluetooth chip it has released since the March 2005 acquisition of wireless-audio-technology vendor Zeevo Inc.

Scott Bibaud, Broadcom's Bluetooth marketing manager, says the BCM2037 leverages Broadcom technology and Zeevo's 4301 Bluetooth chip set. He notes that, by being EDR-functional, the chip now complies with Bluetooth 2.0 plus EDR, tripling its data rate to 3 Mbps from 1 Mbps, previously the highest data rate on a Bluetooth 1.1 platform. The BCM2037 also offers lower power consumption through Bluetooth-based products with its stereo-streaming capability. This process includes transmitting data from host-side, or transmitter, products—such as PDAs, PCs, or cell phones—to stereo headsets on the receiver side. The lower power consumption gives users longer headset-battery life by allowing them to stream data for as long as 10

hours at 3 Mbps, rather than six at 1 Mbps.

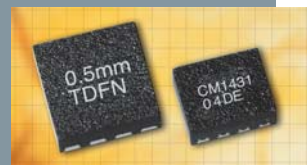
Longer battery life and power-consumption factors are attractive to engineers considering using the BCM2037, and a higher data rate prevents users from hearing sound gaps and data errors. The headset works effectively in longer ranges, because the data moves faster and is more robust. According to Joyce Putscher, director of converging markets and technologies at In-Stat/MDR, the ARM7 processor, which powers the chip, helps expedite the data flow, and many engineers have used it. More important, Putscher notes, is the increased battery life and low power consumption. "When you can design something

that can use a smaller battery, you can potentially reduce design costs, as well as increase battery life," she says. Another advantage is that engineers and designers might be able to design around either a smaller and cheaper battery or provide product differentiation with a longer battery life.

Broadcom's BCM2037 is currently available for sampling to early-access partners and will go into full production during the third quarter. The sample price is less than \$10. This year, Broadcom also released the BCM2045, an EDR chip for cell phones, notebook computers, and other devices. "We are trying to improve the overall user experience by aggressively bringing EDR to the market, as well as improving audio-video-streaming capability," says Bibaud.—**by Jeff Berman**
► Broadcom, www.broadcom.com.

Tiny filter repels EMI/ESD away from wireless functions

As wireless phones get smaller and pack in more auxiliary functions, such as cameras, the potential for EMI problems increases, whereas the space available to squelch these problems shrinks. To address these issues, the Centurion CM1430 and CM1431 filter arrays from California Micro Devices combine EMI



Small—but with big EMI attenuation and ESD protection—the CM1430 and CM1431 filters have a 0.4-mm pitch and a 0.4-mm profile.

filtering with ESD protection in a low-profile, 0.4-mm-high package. These four-, six-, and eight-channel devices implement capacitor-resistor-capacitor pi-filter topologies with cut-off frequencies of 200 and 120 MHz. The CM1430 and CM1431 offer 1-GHz attenuation of 25 and 35 dB, respectively.

ESD protection reaches ± 15 -kV contact discharge, as IEC61000-4-2 Level 4 specifications dictate. Lead pitch is 0.4 mm, compared with 0.5 mm for previous packages. The 0.1-mm difference results in a board-footprint reduction as great as 40%. Devices cost 42 to 59 cents (1000).

—**by Bill Schweber**
► California Micro Devices Corp, www.calmicro.com.

FEEDBACK LOOP

"The problem that engineering work has is really an American societal problem. Jobs that receive the most compensation are generally jobs that deal with money—management, sales, CPAs, bond trader, etc—rather than jobs that create money (engineering, skilled labor, etc). If you want to see the end result of this, study the Roman Empire."

Joel Fields, in *EDN's* Feedback Loop on www.edn.com/article/CA608159. Add your comments.

DILBERT By Scott Adams



Software targets communications design

The Mathworks recently rolled out Communications Blockset 3, an upgraded version of a software program that offers engineers added functions for designing and simulating the physical layer of communications systems and components for wireless and wire-line systems using model-based design. The new version, which includes channel visualization and bit-error-rate-analysis functions, lets users exchange and share executable specifications throughout the modeling and simulation process. These functions allow designers to view various channel-mode-domain behaviors, such as time, frequency, and phasor, to design communications receivers and to compare simulation results with benchmarks in a GUI setting.

Colin Warwick, communications-products manager at The Mathworks, says that Communications Blockset 3 helps improve communications-product design. "Communications products are becoming more computationally intensive than they were in the old days when engineers and designers relied on paper-based models, which were time-consuming and made it hard to 'tease out' de-

sign errors with Spice error codes and netlists," says Warwick.

Model-based design provides a working model of a communications-product design in a test environment to specify a product's behavior before a designer configures the part in hardware or software. "[Engineers and designers] want to focus on building products, not channel models," says Warwick. "This platform prebuilds a wireless channel, letting people focusing on building equalizers and similar products overcome channel impairments." Designing wireless channels is more challenging than building wire-line ones, due to communications products and devices that must adapt to changing landscapes, conditions, and speeds.

The channel-visualization features are particularly helpful for receiver designers, because they let them fix damage that changing conditions cause, says Mike McLernon, senior team leader for communications development at The Mathworks. "When collecting data, channel visualization lets users focus on specific channel characteristics, rather than signal characteristics, such as spreading, 802.11a, or

MOFDM [multilevel-orthogonal frequency-division multiplexing]. This tool can slice into a time or a phasor domain and look at channels at different angles to build receivers that combat the effects of signal characteristics," he says.

The bit-error-rate function lets users working at the physical layer of a design check testbench results against their own work to see where their results should be and how they match up. The tool automates comparisons and simulation results, so that designers can view them in a GUI environment to compare simulations with theory and integrate environments to combine simulation and analysis. This process helps give users a clear indication of when a design is complete by plotting parameters, such as SNR versus bit-error rate.

Communications Blockset 3 also includes a synchronization library, which lets users build receiver models without writing C code and model adaptive and nonadaptive algorithms. The Mathworks' Communications Blockset 3 is now available and costs \$1000. The platform runs as part of the company's flagship applications, Matlab and Simulink.

—by Jeff Berman

► **The Mathworks**, www.mathworks.com.

FEEDBACK LOOP

"We in America are about to discover the harsh reality that our technology is in the heads of the engineers. You lose those heads; you lose the technology. The Chinese realize this. We are in for some very hard times."

Anthony Mendoza, in *EDN's* Feedback Loop on www.edn.com/article/CA526328. Add your comments.



According to the supplier, ATEasy's plug-in fault library and fault editor enable test engineers to develop applications that simplify diagnosis and repair of faults in units under test.

Test executive/development package adds fault library and editor

Geotest-Marvin Test Systems has announced the addition of a fault-library plug-in module and a fault editor to its \$3995 ATEasy 5.0, vendor-independent, open-architecture test executive and rapid-test-application-development software package. According to the company, ATEasy combines the ease of use of Visual Basic with the flexibility of C++. Event-driven programming style maximizes code efficiency, and compiled code speeds program execution. User-defined plain-language commands ease code maintenance, and built-in configuration-management tools simplify project management. Application wizards quickly guide new users through development projects.

The plug-in fault-library software tool facilitates troubleshooting of electronic circuits. The library allows test engineers to create fault dictionaries that provide users of ATEasy applications with simplified diagnostic capabilities. The fault editor allows program developers to define fault conditions that ATEasy will analyze at runtime.

—by Dan Strassberg

► **Geotest-Marvin Test Systems Inc**, www.geotestinc.com.

08.04.05

Q&A

Bob Lucky

Hard work makes its own luck.

Robert “Bob” Lucky, PhD, is the former head of the legendary Bell Labs. Bell was the home of much of the vital research that our industry now employs, including the transistor. It also was the birthplace of some pure research having no apparent application, such as discovering that the omnipresent background noise of the universe is due to remnants of the big-bang theory. While at Bell, Lucky also played a key role in the development of adaptive equalizers’ filtering strategy, a key component in all high-speed modems. He’s also the co-author of the seminal textbook *Principles of Data Communications* and a long-running columnist in *IEEE Spectrum*.

What led you to become an engineer?

A When I was in high school, I didn’t have a clue what engineers did. I was good in math and physics, and I liked to build radios and electronic equipment, so people said I should be an engineer. I marvel at how clueless I was. Now, after a long career as an engineer, I’m still not sure what they do.

I’ll never forget my first week at college. I had to take mechanical drawing, and the instructor told us that all engineers had to start their jobs on the drawing board. That actually wasn’t true even then, but I believed it—especially because I wasn’t much good at mechanical drawing. During a test, I drew something badly, and, in exasperation, I threw my compass down on the drawing. It bounced off the drawing and flew out the open window next to me. I don’t remember how I did on that test, but it couldn’t have been good.

How did you get into writing your *IEEE Spectrum* column and other less-technical items?

A People sometimes ask me how they can get their own column, usually hinting that they could do better than I do. Sometimes, I tell them that you just have to be “lucky.” In the early years of my column, I used to worry that someone would take it away from me. People would send me sample columns that they had written and copy the *Spectrum* editor. That hasn’t happened now for a long time, and, after 23 years of writing the column, I don’t really worry about things like that any more.

I owe the column to the *Spectrum* editor of 1981, who was Don Christensen. He had asked me to do a book review of Tracy Kidder’s *The Soul of a New Machine*—still a great book, by the way—for the institute’s newsletter. They liked my review and asked me to write a movie review of *Tron*.



Then, I wrote a review of Michael Crichton’s *Congo* for *Spectrum*. I was quite abashed when Crichton himself sent a rebuttal to my review to *Spectrum*. I had said that his technology was faulty, and his rejoinder was that his book was fiction, and he could make up stuff. I agreed with this statement but said that the fact that he had included lots of references from *IEEE* journals gave the reader the idea that the technology was correct. In private communication, we both agreed that the other had a point. Moreover, I have to say that his subsequent novels all are based on great technical ideas.

After these reviews, Christensen suggested that I try a column and see how it went. The rest is history. It is truly a great privilege to have a column, and I often take a moment to appreciate the luck and the honor.

In the beginning, I had to submit my columns for clearance through the Bell Labs review process. I was embarrassed to do this, and, apparently, so were the reviewers. Then the public-relations department told me that maybe this clearance wasn’t necessary—that I was on my own for these columns. Now, wherever I go, someone will come up to me and say that they like my columns. I never tire of hearing this, and, whatever work I do on them is worthwhile. People often tell me that I write well

“for an engineer.” I’m never sure whether this is a compliment.

Did you think your work at Bell Labs would have such a broad impact on digital communications?

A Actually, I’ve never thought that my work did have that kind of impact. I was fortunate to be in the right place at the right time, 1961, when modems were first being developed. I’m sure that, if I hadn’t invented the adaptive equalizer, someone else would have done it a month later. Much of technology is like that. There are, of course, exceptions, and the great work of [the late] Claude Shannon, [the “father of information theory”], is the biggest exception to that general rule.

Any comments on the state of engineering and science education?

A People say it’s bad, particularly math education in the secondary schools, but I haven’t been involved in that issue. I have been concerned, however, with what an engineer should learn in college. I’m not sure I have any answers, but I do believe that, in college, you need to learn how to learn, and I’m not sure that this is a real focus. Everything I studied has been obsolete for decades. All that remains is a general engineering culture, some mathematical principles, and an ability to learn new things as time goes along.

—by Bill Schweber

MORE AT EDN.COM

Go to www.edn.com/050804p1 for more from Bob Lucky in an expanded version of this interview.

GLOBAL DESIGNER

Chinese chip vendors push TD-SCDMA terminals

The TD-SCDMA Industry Alliance is this summer sponsoring field tests for TD-SCDMA (time-division synchronous-code-division multiple-access) networks in Beijing and Shanghai. If things go smoothly, separate trial TD-SCDMA-network subscriptions will be available within two to three months after completion of this summer's field tests. Yang Hua, secretary general of the TD-SCDMA Industry Alliance, says that the field tests are focusing on TD-SCDMA-network-infrastructure performance and reliability, interoperability between infrastructures and terminals, and performance of terminals. He adds that the results of these field tests will play a large role in determining whether TD-SCDMA commercialization can become a reality.

However, domestic vendors say that the maturity of TD-SCDMA terminals is the toughest issue for TD-SCDMA's commercialization. "The maturity of TD-SCDMA terminals will not come until mid-2006," says Luo Zhongsheng, assistant general manager of the handset unit of communications-product vendor ZTE (www.zte.com.cn). Chinese terminal-chip vendors, such as T3G (www.t3gt.com), Commit (www.commit.net.cn), and Spreadtrum (www.spreadtrum.com) are cooperating with system vendors to improve the interoperation between infrastructure and terminals.

In April, T3G introduced its chip sets for TD-SCDMA/GSM (global-system-for-mobile-communications) dual-

mode terminals. The company has realized core functions, such as 384-kbps packet-data transfer, 64-kbps real-time circuit-data transfer, and cross-network wandering, through these offerings. T3G officials say that the company's dual-mode chip set interoperates with all TD-SCDMA networks from Datang Mobile (www.datangmobile.com), ZTE, and Putian (www.chinaputian.com). In June, T3G also unveiled an ASIC-based, high-speed PCM-CIA data card, which allows notebook computers to successfully achieve 384-kbps packet-data transfer and conduct broadband multimedia services, such as Internet browsing, FTP downloading, and VOD (voice over data)

through wireless packet networks.

Commit has launched its verified TD-SCDMA-terminal chip set, including baseband, RF, power management, a protocol stack, and a comprehensive development-and-test environment. The chip set supports 3G services, such as video phone, high-speed Internet browsing, and streaming media. Currently, some leading mobile-phone vendors, including LG, Lenovo, and Bird, have introduced their TD-SCDMA mobile phones based on Commit's semiconductor technology. Commit has passed IOT/COT (interoperability tests/continuity tests) on main network equipment from Datang Mobile, ZTE, Putian, and others.

Spreadtrum has also made smooth progress in the development of TD-SCDMA terminals. By teaming up with domestic mobile-phone vendors,

such as Bird, it has developed a host of TD-SCDMA terminals. "The first TD-SCDMA subscribers are more likely to come from the voice market," says Yu Yushu, Commit's chief executive officer. "Data services are certainly important, yet the stable voice services will remain the biggest selling point at the outset." He says that WCDMA (wideband code-division multiple access) has a high place in the market, whereas GSM is on a relatively low level. He believes that TD-SCDMA will emerge in the middle but may be closer to GSM.

—by Harry Wang, EDN China

► **TD-SCDMA Alliance**, www.tdscdma-alliance.org.

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For more global news, visit www.edn.com/global.

LCD driver challenges TFT devices in mobile-phone applications

Targeting mobile phones that rely on color displays, Hong Kong-based Solomon Systech Ltd has launched the first device in a series of innovative CSTN (color supertwist-nematic) LCD drivers. The SSD1784 display controller can support 132×60-pixel-resolution CSTN LCDs. Using the SSD1784, you can achieve 65,000 color combinations in a simple application circuit.

The SSD1784 features a dual OTP (one-time-programmable) ROM, an eight-color power-saving mode, and divider-level accuracy-improvement circuitry. The SSD1784 has more features and uses smaller die than its SSD1783 predecessor and is software-compatible with previous devices from Solomon Systech, which means that designers can reduce development time using the controller.

"CSTN LCDs are catching up with TFT [thin-film-transistor] LCDs in all aspects of display quality, including color depth, contrast, and viewing angle," says Eddy Luk, Solomon Systech's technical marketing engineer. According to Luk, CSTN LCDs also perform better than TFT LCDs in cost and cycle time in mass-production, and, for applications that require no ability to play video, CSTN is a good choice for cost, flexibility, and power consumption.

The SSD1784 offers partial-, sleep-, and eight-color standby modes. When you invoke the eight-color mode, the display controller's frame-rate control and PWM circuitry partially turn off. These circuit blocks generate gray-scale levels for RGB signals. Circuitry on the controller allows you to display red, green, blue, cyan, yellow, magenta, black, and white colors.

—by NS Manjunath, EDN Asia

► **Solomon Systech Ltd**, www.solomon-systech.com.



The SSD1784 display controller can support 132×60-pixel resolution CSTN LCDs and achieve 65,000 color combinations in a simple application circuit requiring a microcontroller.

08.04.05

pulse

INNOVATIONS AND INNOVATORS

6 GHz spectrum analyser mixes production and portable roles

Rohde & Schwarz has added the model FSL into its line-up of spectrum analysers; intended as a budget instrument with a comprehensive feature set, it comes in four models that range up to 3 or 6 GHz and have the option of a tracking generator. I/Q demodulation band-width is 20 MHz (sufficient, its designers say, for work on wireless LAN projects), and the displayed average noise level in a 1 Hz bandwidth is -152 dBm. Total measurement uncertainty is under 0.5 dB. Phase noise is -103 dBc in 1 Hz, 10 kHz from a carrier. Users can connect the instrument directly to high-level signals without external attenuators—its 1-dB compression point is at +5 dBm.

The FSL is intended both for bench and production environments, with a measurement speed of over 80 sweeps/sec, and electronic attenuators to speed set-up changes and eliminate wear. It includes R&S's "fast ACP" measurement routine to determine adjacent-channel power with a time-domain technique. The instrument's designers have made extensive use of digital filtering, and have included a 10/1000 BaseT LAN port for data transfer. Users can also operate the FSL for up to one hour from an internal battery supply. Price point for the analyser



The FSL spectrum analyser includes much of the measurement feature set from R&S's high-end series instruments.

is from just under €11,000 to €16,500, depending on specification.

In the field of network analysis, R&S has extended the concepts behind its ZVB family of instruments (4 and 8 GHz network analysers) into the microwave spectrum. The ZVB family introduced the architecture of a separate generator (source) for each of the ports on the unit, with continuous monitoring to ensure that the multiple sources remain locked and levelled. Each port also features an independent receiver, so that each has a separate reflectometer function. This speeds up measurement by removing the need for extensive internal switching to set the instrument up, and simplifies the task of providing "one-button" reporting of, say, complete S-parameter sets. With the new models in the family, the frequency range is extended to 20 GHz—first in a 2-port version, and later in 3- and 4-port variants. A Windows-based instrument, the ZVB20 can output 16 dBm on all ports, with a power sweep range of over 50 dB. Dynamic range is quoted as over 123 dB. Users can control the unit either from the Windows interface, or by hard- and soft-keys. In the Windows interface, menus are context-sensitive to the current measurement set-up.

—by Graham Prophet

▷ **Rohde & Schwarz**,
+49 89 412911765,
www.rohde-schwarz.com.

Processor modeling supports concurrent development

Concurrent design has long been an objective of vendors supplying development tools to the embedded design community. Designers could greatly speed up the design process if they could develop embryonic code on a virtual model of the final hardware, without software de-signers having to wait for a physical prototype of the system to be built. To develop useful software, the virtual representation of the hardware has to be accurate (preferably completely cycle-accurate): but a detailed model of a hardware system written in conventional language will run too slowly for code developers to do useful work. To get usable speed, tool vendors must employ some sort of abstraction of hardware behaviour. The effort to achieve a truly useful compromise between speed and accuracy has been the story of this branch of the EDA industry.

Currently claiming to have squared that circle is VaST Systems, justifying its assertions with a user list that includes many automotive- and consumer-product builders, especially in the Japanese market. VaST's tools model processors and other hardware—the company quotes cycle-accuracy of typically 97-98% for models that run at 40 MIPs on standard computer hardware (no hardware acceleration is involved). Underlying the tools is a proprietary modeling language—but this is hidden from the user, who sees a shell around device models in

standard C. In the tool set, CoMET is an architectural exploration tool that—among other functions—allows system architects to develop virtual system prototypes from higher level representations, following an “executable specification” approach. The other major tool is METeor, a software development environment that hosts code on the virtual prototypes.

VaST is now engaged in making the technology for creation of models in its system more widely available. The process started with the release of a platform-creation tool which enabled users to assemble a system model from library blocks; and a peripheral device builder, that lets users create functions at that level. VaST is not yet ready to release tools that will enable users to model a complete processor—that capability will follow later—but the company's latest announcement is a “virtual processor model transformer”. This tool will allow users to modify the instruction set of a “seed” virtual processor that the company supplies. A seed would comprise instruction set, micro-architecture, pipelining and other essential behavioural data. Developers apply the “transformer” tool to the model to add, modify or remove instructions. At a cost of \$100,000 for a one-year licence, this is clearly not a tool for every user—VaST is attempting to proliferate the ability to produce models for processor variants into end-

users who are in a position to build SoC ASICs, and into silicon-vendors with processor product lines. The company's aspirations are that their models become a routine deliverable along with a given processor variant.

At the end-user level, the VaST tool set has an entry point that is also around the \$100,000 level—the CoMET tool costs \$30,000 per seat,

for example—and CEO Alain Labat acknowledges that “a certain level of complexity” is needed to justify use of the software. Models are available for processors from a list of sources that includes ARM, Intel, NEC, MIPS, Renesas, Freescale, Toshiba, DSP Group, and StarCore.

—by Graham Prophet
 ▶ VaST, +44 1296 713113, www.vastsystems.com.

Programmable array develops magic touch

Cypress Semiconductor has produced an optimised application for its PSoC configurable silicon product that carries out the sensing function in capacitive, touch-sensitive switches. PSoC is a programmable part that includes a small microcontroller core, non-volatile memory, SRAM and an array of programmable logic and programmable analogue and mixed-signal functions. The CapSense product integrates all of the circuitry that is needed to provide capacitive-based touch-activated switching, yielding a large saving on parts-count over other implementations. For each circuit the chip senses, the proximity of a finger alters the capacitance between two plates, which are themselves behind a non-conductive panel. There is no electrical contact between the activating touch and the circuitry—in fact, the isolation barrier can be of substantial plastic or glass. The capacitor is part of the frequency-setting loop of a relaxation oscillator. On-chip circuitry gates and counts the oscillator's output and uses the altered count as the detected signal. Designers can use CapSense to detect simple switch (on/off) actions, or finger-activated “slider” setting of a variable level according to where a fingertip touches or slides along a scale. A single IC can sense as many as 48 switch lines, and can host integral LED/LCD drivers, signalling output data via I²C or SPI interfaces. The 8-bit microcontroller in the PSoC, and the SRAM on-board, have sufficient free capacity to also host simple control applications, further reducing the bill-of-materials in applications such as complex front-panel design. In quantity, the chip will sell for under \$1.00; demonstra-



A single mixed-signal programmable device can sense up to 48 lines.

tion kits illustrate front-panel design and slider configurations, and the company supplies complete source code.

—by Graham Prophet
 ▶ Cypress Semiconductor, +44 1279 873160, www.cypress.com.

GLOBAL DESIGNER

“Pre-n” WiFi chip set implements full MIMO proposal

Observers of the technologies that will underpin the wideband domestic environment of the near future largely agree that there will be a need for some form of broadband backbone for the home. Opinions vary on whether it will be wired or wireless, and on which standards will prevail. Israeli silicon supplier Metalink believes that the solution will be Ethernet-based, specifically the 802.11n variant of the WiFi standard. 802.11n is still some way from being a ratified standard; Metalink is one supplier to the emerging “pre-n” market of equipment. Companies participating in this sector bring product to market ahead of ratification of the standard, using their own estimates of what the final version will contain. At the same time, Metalink’s chip set retains backward compatibility with existing WiFi standards such as -b and -g.

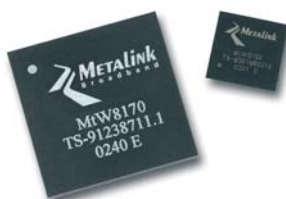
The company offers a chip set for the MIMO (multiple-input, multiple-output) technology that transmits multiple carriers with separate encoded data streams over the same RF channel to increase channel capacity. MIMO relies on multipath propagation between transmitter and receiver to add differentiation to the two (or more) signal streams. This enables the receiver to separate the original data,

albeit with considerable baseband processing. Barry Volinskey, Metalink’s Associate Vice President, strikes a note of realism about “on-the-box” WiFi data rates. The typical -g product might quote 60 Mbps, while actually achieving perhaps 20 Mbps over short distances. Metalink’s implementation of early-n technology achieves, he claims, a true rate of 60 Mbps at 20m range—sufficient for two HDTV bit streams. Metalink’s chip set comprises an RF chip, already sampling, and a baseband part, due out in September. The Mtw8150 RF part integrates two transmit/receive paths on a single chip and can be used with, or separately from, the forthcoming baseband part. It requires an external power amplifier, but no separate low noise amplifiers, filters or other functions. Metalink’s designers employed silicon-germanium technology to achieve the required performance at 5 GHz, the band that Metalink has chosen to employ. It is, the company says, the only product so far announced that combines MIMO with the use of 40-MHz channel width (through “bonding” of 20 MHz channels).

The baseband part (8170) will be in 0.13-micron CMOS, supporting 2×2 or 2×3 MIMO schemes, and presenting a complete access point. It will support raw PHY bit rates of 243 Mbps with 40 MHz channel bonding, or 135 Mbps using 20 MHz channels.

—by Graham Prophet

► **Metalink,**
+972 9 960 5555,
www.metalinkBB.com.



Supercaps packaged for high-energy storage tasks

Designers using supercapacitors for energy storage in systems such as hybrid or all-electric vehicles, or in power generators such as wind turbines, now have the option of a 6-cell module that offers a working voltage of 16.2V. The working voltage of almost all such dual-layer capacitor technologies has been limited to 2.5V,



Maxwell’s latest ultracapacitors come pre-packaged for incorporation into energy-storage applications.

and improvements have been difficult to achieve. Maxwell Technologies’ 2,600F MC2600 Ultracapacitor uses a new construction that pushes the operating voltage to 2.7V, or 16.2V for the series-connected BMOD2600 module. The total capacitance of the module (six series connected capacitors) is 430F; there is active balancing between each of the cells in the pack. The six-cell pack measures 420×160×70mm and costs €366 in medium volumes (€54 per cell in similar volumes). —by Graham Prophet
► Maxwell Technologies,
+41 26 4118500,
www.maxwell.com.

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