

## Dither a power converter's operating frequency to reduce peak emissions

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Designers of dc/dc switching power converters face the challenge of controlling EMI (electromagnetic-interference) emissions produced during normal operation. If large enough, these emissions conduct through power lines or radiate to other assemblies within a system and can compromise a system's performance. Emission peaks typically occur at the converter's fundamental switching frequency and gradually reduce in amplitude at each higher order harmonic, with most of the emitted energy confining itself to the fundamental and lower order harmonics. Modulating, or dithering, the power converter's operating frequency can reduce the peak emissions by spreading EMI over a band of frequencies.

Most modern PWM controllers use an external resistor to set the operating frequency, which typically increases with decreasing resistor values. For

example, the LM5020's internal oscillator delivers a regulated 2V at its programming pin (RT), and a programming resistor connected to RT sets the current that RT delivers. The oscillator also delivers a proportional current into an internal timing capacitor (Reference 1). The period of the timing capacitor's ramping voltage determines the oscillator's frequency.

The external dithering circuit in Figure 1 comprises a simple stand-alone comparator-based oscillator configured to operate at approximately 800 Hz. The output state of comparator IC<sub>2</sub> goes high upon power-up. R<sub>1</sub>, R<sub>2</sub>, and R<sub>3</sub> set the comparator's positive input, which initially rests at 2.9V. The voltage at capacitor C<sub>3</sub> ramps up toward the positive threshold.

When the voltage at the comparator's negative input reaches the positive-threshold voltage, the comparator's output switches low, which also

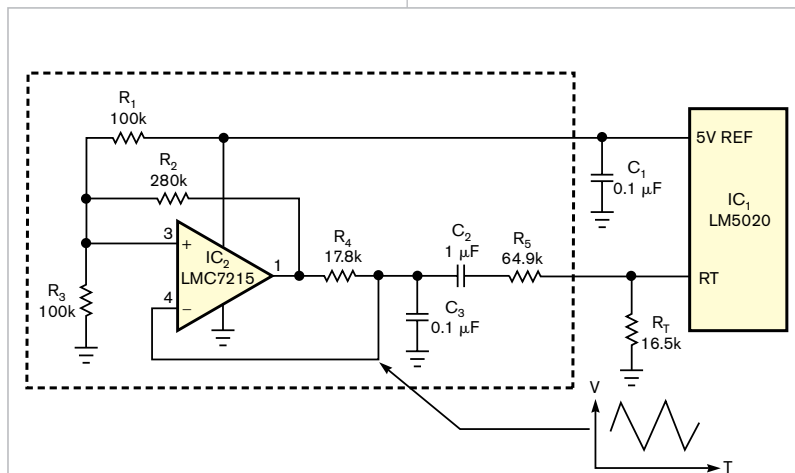


Figure 1 A low-frequency triangular-wave oscillator modulates a PWM controller's oscillator frequency.

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lowers the threshold at the comparator's positive input to 2.1V. The voltage at capacitor C<sub>3</sub> then ramps down toward the new threshold, and, when it reaches the lower threshold voltage, the cycle repeats. The voltage across C<sub>3</sub> approximates a triangular wave with a minimum voltage of 2.1V and a maximum of 2.9V.

To dither the LM5020 controller's PWM-oscillator base frequency, the triangular wave generated by IC<sub>2</sub> modulates the current from the controller's RT pin. Resistor R<sub>5</sub> sets the percentage of modulation dither. The right side of R<sub>5</sub> is fixed at the RT pin's regulated potential of 2V, and the low-frequency triangle wave coupled from IC<sub>2</sub> through capacitor C<sub>2</sub> drives R<sub>5</sub>'s left side. For R<sub>5</sub> with a value of 64.9 kΩ, the peak-to-peak current through resistor R<sub>5</sub> is approximately 12 μA. With the dither circuit disconnected, the steady-state current that RT sources is approximately 121 μA, and the 12-μA p-p dither current thus represents 10% total modulation.

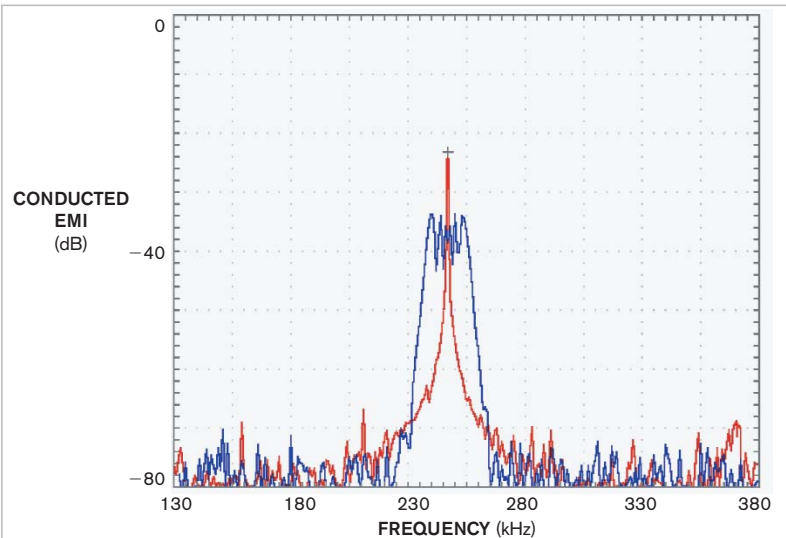
An LM5020-controlled PWM fly-back dc/dc converter, IC<sub>1</sub>, evaluates the dither circuit's effectiveness. The circuit's fundamental operating frequency is 250 kHz, which the controller's R<sub>T</sub>

resistor sets. The red trace of **Figure 2** shows the conducted emissions on the circuit's positive input-power line without the dither circuit in operation. The peak emissions are narrowly confined around the fundamental oscillator frequency of 250 kHz with a measured amplitude at the fundamental frequency of  $-24$  dB.

Connecting the dither circuit to the controller's RT input produces the blue trace of **Figure 2**. Conducted emissions around the fundamental frequency now disperse around the fundamental frequency with maximum amplitude reduced by  $-34$  to  $+10$  dB. **EDN**

## REFERENCE

1 LM5020 data sheet, National Semiconductor, [www.national.com/pf/LM/LM5020.html#Datasheet](http://www.national.com/pf/LM/LM5020.html#Datasheet).



**Figure 2** Measured at the dc/dc converter's input, peak conducted emissions without dither (red trace) decrease by 10 dB with dithering applied (blue trace).

## Single-port pin drives dual LED

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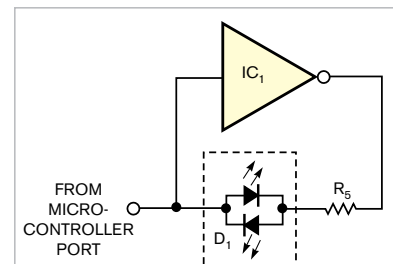
Most current microcontrollers offer I/O ports that can change their functions during program execution. As outputs, the circuits can sink and source reasonably large amounts of current. This Design Idea shows three alternative methods for driving a two-pin, two-color LED from a single I/O pin. **Figure 1** illustrates one possible approach that uses external inverter  $IC_1$  to drive  $D_1$ , a red/green bidirectional LED. A logic-high output on the port pin forces current through the green (upper) LED and pulls the inverter's input high, which drives the inverter's output low and sinks current from the green LED. A logic-low output on the port pin raises the inverter's output high, delivering current to the red (lower) LED; the microcontroller's output sinks current from the red LED.

To turn off both LEDs, you reconfigure the microcontroller's port pin from output to input or switch the pin to tri-state mode, either of which prevents the microcontroller's port pin from

sourcing or sinking current. This circuit's primary disadvantage is that it yields no control over each LED's brightness; instead, resistor  $R_5$  determines forward current for both LEDs.

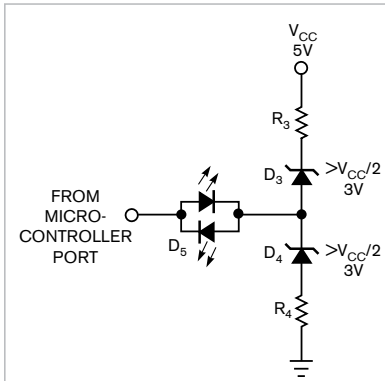
**Figure 2** presents an approach that also involves a major disadvantage. Zener diodes  $D_3$  and  $D_4$  and resistors  $R_3$  and  $R_4$  form a low-impedance voltage divider that applies  $V_{CC}/2V$  to one end of LED  $D_5$ . The value of  $V_{CC}$  drives the selection of the zener diodes' voltage,  $V_Z$ , with lower voltage zener diodes allowing more LED current and higher voltage ones limiting maximum LED current. Given that the microcontroller's outputs can deliver rail-to-rail voltages, the difference between  $V_{CC}$  and  $V_Z$  limits maximum forward current for both LEDs. For example, if  $V_{CC}$  is 5V and  $V_Z$  is 3V, the forward voltage across either LED is less than 2V. Once a designer selects the zener-diode voltage, only small variations in  $V_{CC}$  can occur; otherwise, the LEDs' brightness would fluctuate.

Using discrete components, another circuit offers an inexpensive approach that avoids the other circuits' disadvantages (**Figure 3**). When the microcontroller's output port goes high, current flows through the green (upper) LED,  $R_2$ ,  $D_2$ , and FET  $Q_2$ , which the port's high level turns on. When the microcontroller's output port goes low, transistor  $Q_1$  turns on and delivers current to the port pin through  $R_2$  and the red (lower) LED. The circuit operates symmetrically because silicon diode  $D_2$ 's forward-voltage drop is present



**Figure 1** An inverter can drive a bidirectional, two-color LED but applies the same amount of current to both LEDs.

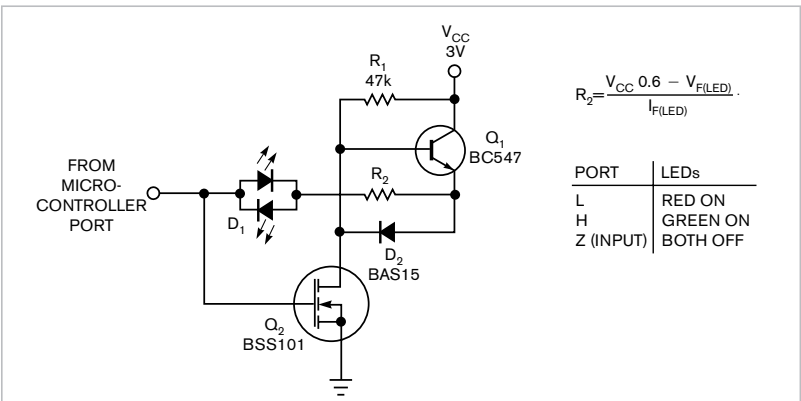




**Figure 2** A zener-diode and resistor-voltage divider exhibits sensitivity to supply-voltage variations and allows LED brightness to vary.

regardless of whether the microcontroller's port pin goes high or low.  $V_{CC}$  may vary during operation but must remain higher than 3V.

You can individually adjust the LEDs' currents to equalize brightness or compensate for a difference between the microcontroller's power-supply voltage



**Figure 3** This circuit provides immunity to supply-voltage fluctuations and more uniform LED brightness.

$$R_2 = \frac{V_{CC} 0.6 - V_{F(LED)}}{I_{F(LED)}}$$

PORT	LEDs
L	RED ON
H	GREEN ON
Z (INPUT)	BOTH OFF

and the LED-driver circuit's  $V_{CC}$ . Replace  $R_2$  with two resistors connected in series between  $Q_1$ 's emitter and  $D_2$ 's anode. Connect the midpoint of the two resistors to the LEDs.

With the microcontroller's port pin configured as an "input with pullup," the port delivers a small current to the green LED. However, pullup-resistor

values of 22 k $\Omega$  or higher do not cause misleading light output from LEDs in the off-state. When the input signal from the port pin floats—that is, with  $V_{CC}$  at 5V and the port configured as an input with no pullup resistor—the circuit draws no additional current, and the quiescent current, which  $R_1$  determines, averages less than 100  $\mu$ A. **EDN**

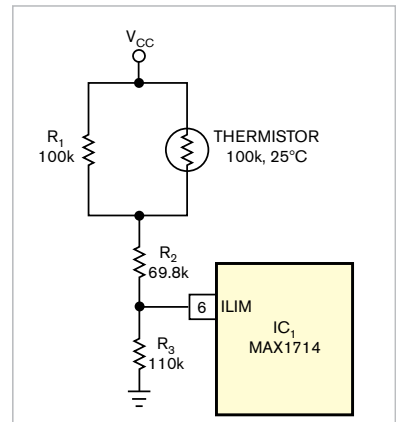
## Network linearizes dc/dc converter's current-limit characteristics

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Recently announced versions of integrated step-down dc/dc converters have eliminated the requirement for a high-side current-sense resistor by sampling the voltage drop across an external, low-side, MOSFET synchronous rectifier. This topology eliminates the sense resistor's cost and pc-board-space requirement and also provides a modest increase in circuit efficiency. However, the MOSFET's highly temperature-dependent on-resistance dominates the current-limit value. Fortunately, certain newer dc/dc converters, such as Maxim's MAX1714, allow external adjustment

of the current-limit threshold. The circuit in **Figure 1** shows how a thermistor applies temperature compensation to the circuit's output-current limit.

The MAX1714's linear current-limit ( $I_{LIM}$ ) input range at Pin 6 of IC<sub>1</sub> spans 0.5 to 2V, which corresponds to current-limit thresholds of 50 to 200 mV, respectively. For the default current-limit setting, 100 mV, the circuit imposes a 7.5A current limit at 25°C. However, **Figure 2** shows that the current limit varies from 9A at -40°C to 6A at 85°C. To design the temperature-compensation network, begin by breadboarding the circuit and using an



**Figure 1** A thermistor-resistor network provides temperature compensation for a dc/dc converter's current-limit input,  $I_{LIM}$ .

external power supply to vary the MAX1714's current-limit input voltage such that the output-current-limit value remains constant. You repeat the



measurements at 10°C intervals over the circuit's operating-temperature range.

To compensate for IC<sub>1</sub>'s temperature variation, you can select from among several possible resistor-thermistor-network topologies. First, you need to select a suitable thermistor and characterize its resistance-versus-temperature variation. Because the MAX1714's current-limit input pin feeds a relatively high input-impedance voltage-follower stage, this thermistor requires a high nominal resistance of 100 kΩ. Resistance-versus-temperature characteristics of inexpensive thermistors exhibit considerable nonlinearity, but one relatively simple approach to linearization involves paralleling the thermistor with a fixed resistor equal to the thermistor's nominal resistance (Reference 1). In the network of Figure 1, R<sub>1</sub> linearizes the thermistor, and R<sub>2</sub> and R<sub>3</sub>, respectively, set the slope and intercept of the current-limit-voltage-versus-temperature-characteristic curve.

To arrive at optimal values for R<sub>2</sub> and R<sub>3</sub>, we prepared a spreadsheet incorpo-

rating the original current-limit-voltage-versus-temperature data and added columns for each of the network's resistors, plus the thermistor specification sheet's resistance-versus-temperature data. While observing the circuit's temperature-versus-voltage transfer function, we varied the spreadsheet's values for R<sub>2</sub> and R<sub>3</sub> until the transfer function best approximated the measured current-limit-voltage-versus-temperature data. Finally, we constructed the circuit and tested it over the temperature range and noted that it yielded a reasonably flat response.

The curvature of the corrected output characteristic of Figure 2 (red trace) is intrinsic to the thermistor. Though not perfectly flat, the corrected curve represents a great improvement over the original (black trace) and is sufficient to meet the original

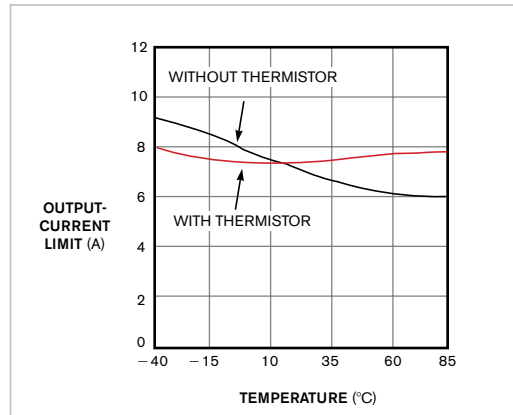


Figure 2 Before (black trace) and after (red trace) current-limit-versus-temperature characteristics show the performance enhancement that the circuit in Figure 1 provides.

design goal. You can achieve more precise compensation by selecting a different thermistor or by incorporating multiple thermistors.EDN

REFERENCE

1 Horowitz, Paul and Winfield Hill, *The Art of Electronics*, ISBN 0 521 37095 7, Cambridge University Press, New York, 1980.

## Add a Schmitt-trigger function to CPLDs, FPGAs, and applications

Stephan Roche, Santa Rosa, CA

Thanks to its internal hysteresis, the highly useful Schmitt-trigger circuit accepts a low-slew-rate input signal and produces a clean, glitch-free output transition. Unfortunately, user-programmable logic devices, such as CPLDs and FPGAs, generally offer no direct method of synthesizing Schmitt-trigger gates and buffers. This Design Idea shows how a few external components and some VHDL code can implement a Schmitt trigger and put it to work in several useful applications.

To create an equivalent of the basic Schmitt-trigger buffer, you use two external resistors to create positive feedback around a buffer (Figure 1a and b). You can also use four external resistors to set two threshold levels around an R-S flip-flop (Figure 1c).

The following equations, respectively, describe the basic Schmitt trigger's positive- and negative-threshold levels:

$$V_+ = \frac{R_1}{R_2} V_{CC} + V_{TH} \left( 1 - \frac{R_1}{R_2} \right);$$

$$V_- = V_{TH} \left( 1 - \frac{R_1}{R_2} \right).$$

In these equations, V<sub>TH</sub> represents the input-voltage threshold of the CPLD/FPGA device, and V<sub>CC</sub> is its power-supply voltage.

Based on the equivalent Schmitt-trigger circuit in Figure 1b, the low-cost resistance-capacitance oscillator in Figure 2 requires four external passive components. Resistor R and capacitor C set the circuit's oscillation frequency. Note that the resistance values of R<sub>1</sub>

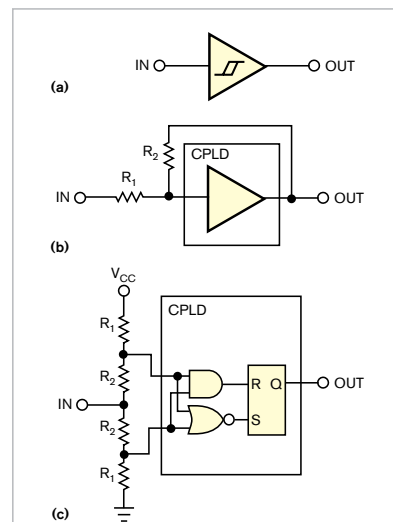


Figure 1 Use a portion of a programmable-logic device or gate array to implement a Schmitt-trigger buffer (a) by adding either two (b) or four external resistors (c).



and  $R_2$  must be larger than that of  $R_1$ . **Listings 1** and **2** contain the circuit's VHDL implementation and RTL architecture, respectively.

In **Figure 3**, an open-collector buffer provides the trigger for the basic Schmitt-trigger-retriggerable monostable circuit by discharging timing capacitor  $C$ . The circuit's output pulse width approximately equals the time constant  $RC$ . **Listing 3** shows the VHDL implementation and RTL architecture, respectively.

You can convert the retriggerable monostable into the nonretriggerable monostable in **Figure 4** by using an open-collector NAND gate to discharge timing capacitor  $C$ . As long as the circuit's output remains high during the timing interval, the system locks out external triggers. As in the previous circuit, the output pulse width approximately equals the time constant  $RC$ . **Listing 4** contains the VHDL and RTL codes.

You can use the basic CPLD buffer-with-feedback circuit to provide hysteresis for a contact-debouncing circuit. In **Figure 5**, resistor  $R_4$  provides contact-cleaning current, and  $R_3$  and  $C$  form a low-pass filter to reduce noise that contact bounce generates. Component values vary depending on the application. **EDN**

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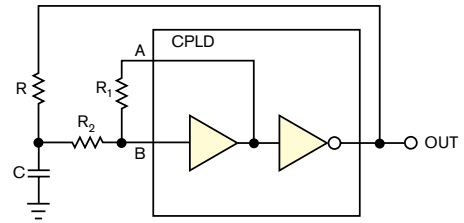
Entity Oscillator is
  Port (
    A : in std_logic;
    B : in std_logic;
    OUT : out std_logic
  );
end Oscillator;

architecture RTL of Oscillator is
begin
  A <= B;
  OUT <= not A;
end RTL;

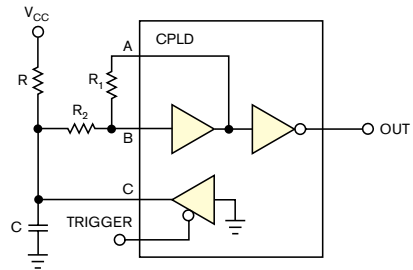
Entity Monostable is
  Port (
    A : in std_logic;
    B : in std_logic;
    Trigger : in std_logic;
    C : out std_logic;
    OUT : out std_logic
  );
end Monostable;
architecture RTL of Monostable is
begin
  A <= B;
  OUT <= not A;
  C <= '0' when Trigger='1' else 'Z';
end RTL;

Port (
  A : in std_logic;
  B : in std_logic;
  Trigger : in std_logic;
  C : out std_logic;
  OUT : out std_logic
);
end Monostable;
architecture RTL of Monostable is
begin
  A <= B;
  OUT <= not A;
  C <= '0' when Trigger='1' and A='0' else 'Z';
end RTL;

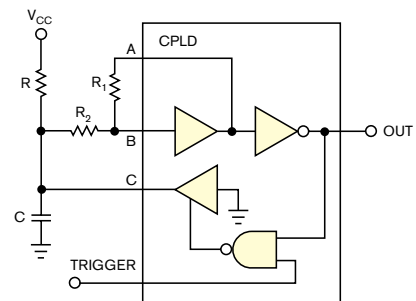
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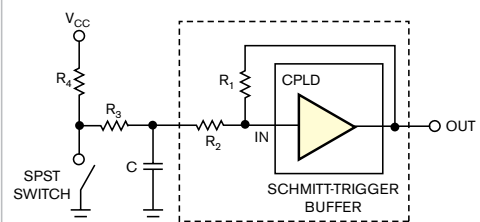
**Figure 2** Add a resistor and capacitor to a basic Schmitt-trigger buffer to form a low-cost oscillator.



**Figure 3** An active-low buffer holds timing capacitor  $C$  discharged in this version of a retriggerable monostable multivibrator based on the Schmitt-trigger buffer.



**Figure 4** A NAND gate locks out trigger pulses, forming a nonretriggerable, monostable circuit.



**Figure 5** Use a Schmitt trigger to debounce switch contacts.