

leading edge

What's hot
in the
design
community

Edited by
Fran Granville



Engineered into the genes

"All children are born as engineers. Watch them at play. They're not just playing. They're building and learning. They are engineering. Then we spend years squashing it out of them."

**—Geoffrey Orsak,
dean of engineering,
Southern Methodist
University**

Reference design delivers low-cost Bluetooth access point

By Warren Webb

CAMBRIDGE CONSULTANTS has unveiled a reference design for a Bluetooth cordless-telephony access point with a bill of materials of less than

\$15. The design allows users to employ mobile handsets with Bluetooth as three-way devices. They can make calls on the cellular network when roaming, but, when users are in range of an access point, Bluetooth provides a cordless connection to the fixed network. The reference design is for a single-line telephony-access point for residential applications and is available ready for manufacture with schematics, pc-board files, and software for a one-time license fee or per-unit royalties. Tim Whittaker, a consult-

ant at Cambridge Consultants explains, "With this design, we have stripped a very significant amount of cost from the usual bill of materials, as well as reducing pc-board size and power consumption." The company built the Bluetooth telephony-access point on a single-chip BlueCore2 device and its on-chip XAP microcontroller, with a power amplifier to achieve Class 1 performance and support a range of 100m. The design uses external flash memory for the application program and a low-cost external codec for



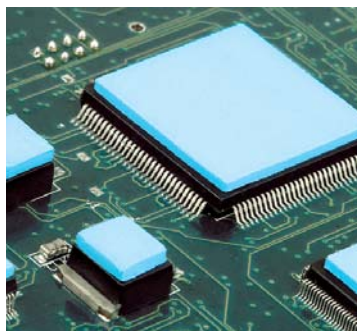
A new reference design provides wireless-mobile-phone connection to the public-switched-telephone network via Bluetooth access points.

the Bluetooth-to-PSTN interface. The design is implemented on a pc board measuring 1.6×2.3 in.

► **Cambridge Consultants Inc.**, www.cambridgeconsultants.com.

Keep cool by conforming

IT'S VITAL TO MAINTAIN tight thermal coupling between an IC and its heat sink, and a new group of thermal pads from Bergquist offers conductance along with conformability; you can even use these pads so a single sink can bridge several ICs. The S-Class series of gap pads, comprising the 2000S40, 2500S20, and 3000S30, have thermal conductivity of 2, 2.4, and 3W/m-K (watts per meter Kelvin), respectively. The pads' 20, 40, or 30 bulk hardness on the Shore 00 scale allows them to better conform to the surface of an IC and the heat sink above it. The laminated pads have a resin formula-



Keep one or more ICs thermally coupled to a heat sink using the S-Class family of compliant, conductive gap pads.

tion with embedded-glass reinforcement at the top to resist punctures and tears, and a lower, tacky, rubberlike surface. These pads need no additional adhesive, which might impede heat flow.

Designers can choose their combination of conductivity and compliance. The pads are available in sheet or die-cut form in thicknesses of 10 to 125 mils; a 1×1-in., 20-mil pad costs 19 cents to 42 cents (2500), depending on the version.

—by Bill Schweber

► **Bergquist Co.**, 1-800-347-4572, www.bergquistcompany.com.

6U-high FPGA-based analyzers reduce 2G-sample/sec data as fast as it arrives

SAYS PHIL GREGOR, product manager at Acqiris, which manufactures modular, high-speed data-conversion instruments, “Acquiring

long records of wide-bandwidth analog signals at rates as high as 2G samples/sec is only part of the problem that many engineers who deal with such signals have to solve.” To be useful in real-time applications—which range from radar-signal processing, mass spectrometry, and millimeter-spectroscopy analysis, to

acoustic microscopy and interferometer-signal processing—he says, many setups that perform direct sampling must filter and reduce the data as rapidly as it arrives. Such setups often require greater processing speed than familiar computing architectures can provide. Although FPGA-based analyzers that offer the necessary speed have existed for several years, they haven’t offered the user programmability that many applications require.

To provide both the speed and the programmability, Acqiris now offers dual- and single-channel 6U CompactPCI high-speed analyzers that capture and perform synchronous real-time signal processing at rates to 2G samples/sec. The AC240 and AC210 analyzers each host a reconfigurable onboard data-processing unit, making them ideal for real-time operations on high-speed digitized signals.

For users who wish to implement proprietary processing algorithms, Acqiris offers a firmware-development kit that defines the architecture and provides the basic framework for programming the FPGA-based data-processing units.

Each analyzer-input channel includes a 1-GHz-bandwidth front end with full signal conditioning and calibrated gain and offset ranges. The high-performance AC240 includes two synchronous channels, each with a 1G-sample/sec ADC. For single-channel applications, you can interleave these ADCs, doubling the maximum sampling rate to 2G samples/sec and improving the overall timing resolution. The lower cost AC210 includes a single channel with a maximum sampling rate of 1G samples/sec.

The data-processing unit on the two analyzers, a Virtex II Pro 70 FPGA, executes multiplications in less than 5 nsec and offers more than 74,000 logic cells, 328 dedicated 18×18-bit multipliers with 36-bit results, and nearly 7 Mbits of on-chip processing

memory. Acqiris also offers an optional onboard processing-memory extension, providing as much as 512 Mbytes of onboard SDRAM and 2 Mbytes of dual-port SRAM with a read/write throughput as high as 2 Gbytes/sec to and from the FPGA. Prices for AC240 and AC210 analyzers start at \$18,990.

Acqiris is now also offering the AcqirisMAQS stand-alone multichannel-acquisition-software package. The package, which simplifies monitoring and control of advanced multichannel data-acquisition systems, enables the remote operation of multiple systems at various locations. AcqirisMAQS targets use in applications such as astrophysics and high-energy physics, which require large numbers of channels.

The package integrates a remote-control interface that allows simultaneous control and monitoring of data-acquisition systems from multiple locations and lets you access test systems at dispersed sites. With AcqirisMAQS, you can use any desktop or laptop PC as an interface terminal to control multiple digitizer channels via an Ethernet connection or a simple crossover cable in on-site or remote Ethernet-based network environments. Prices for AcqirisMAQS start at \$1990 for a single-user PC license. A free demo version of the software is available.

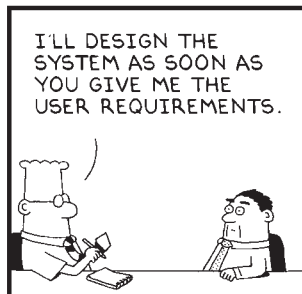
—by Dan Strassberg

► Acqiris USA, 1-877-227-4747, www.acqiris.com.



The 6U-high AC210 and AC240 FPGA-based analyzers in real time filter and reduce data they acquire at rates as high as 2G samples/sec.

DILBERT By Scott Adams



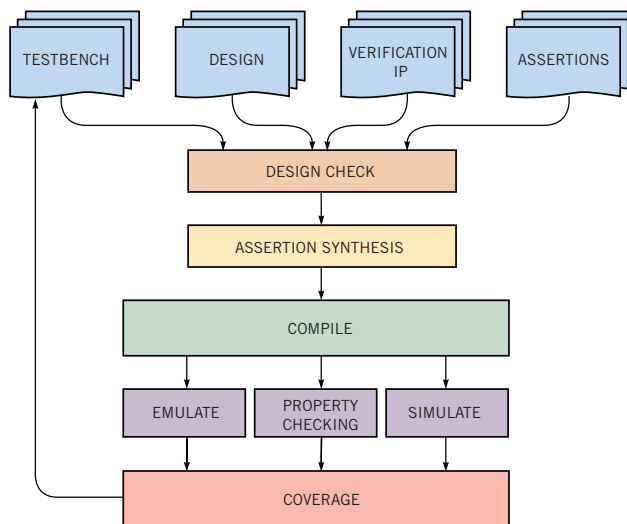
► The use of robots around the house to mow lawns, vacuum floors, pull guard duty, and perform other chores is set to surge sevenfold by 2007, according to a survey by the UN Economic Commission.

Tool combines coverage-driven, assertion-based verification

MENTOR GRAPHICS has released a version of ModelSim that integrates the technology the company recently acquired with the purchase of

0-In Design Automation. ModelSim 6.0 offers standards-based support for assertion-based and coverage-driven verification. Mentor based the Scalable Verification product on the ModelSim simulation environment that supports Verilog 2001, VHDL, PSL, SystemC, and SystemVerilog. The newly integrated native assertion engine and assertion debugging increase designers' efficiency in testing designs. The functional-coverage capability allows

engineers to track the effectiveness of the verification efforts. ModelSim 6.0 improves the integration with the Seamless Co-Verification Environment, the Vstation family of emulators, and the Advance MS analog/mixed-signal simulator. List prices for ModelSim Version 6.0 begin at \$4495.—by Gabe Moretti
►Mentor Graphics Corp, 1-503-685-8000, www.mentor.com.



ModelSim integrates functional-coverage capability that allows engineers to track the effectiveness of their verification efforts.

Graphite spreader diffuses thermal woes

A DESIGNER'S CHALLENGE is not only to remove heat from the component that is dissipating it, but also to get that heat to where he wants it to go. The conventional approach is to employ a copper or an aluminum heat spreader, often coupling it with a heat pipe or a fan, but the SpreaderShield from GrafTech International Ltd offers a passive alternative with lower weight plus directed heat flow.

Made of graphite fibers, this pliable spreader is anisotropic, conducting heat well along its x and y axes but poorly in the z axis. As a result, it conducts the heat longitudinally away from the source. Several laptop PCs and cell phones use the material to spread CPU-heat dissipation toward the case corners and thus minimize hot spots, notes Julian Norley, PhD, director of technology at the company, adding that the SpreaderShield



Direct heat away from its source by using GrafTech's graphite thermal spreader, which offers anisotropic thermal conductivity, along with lower weight than copper or aluminum.

conveys the heat to the case over an area much broader than the IC's footprint alone. Designers can also apply the material to large systems, such as big-screen, plasma TVs, to eliminate hot spots, which the image and color on screen can cause.

The in-plane 2-D thermal conductivity of the material is as high as 500W/m-K (watts per meter Kelvin)—comparable with copper and twice that of aluminum—and the z-axis conductivity is less than 10W/m-K. The SpreaderShield material weighs approximately 30% less than aluminum and 80% less than copper, and designers can coat the material with a thin metal layer for EMI shielding, as well. Cost depends on size and final form factor but is typically a few dollars per unit (volume quantities).—by Bill Schweber
►GrafTech International Ltd, 1-302-778-8227, www.graftech.com.

►About 80% of people 19 to 65 own cell phones, and more than 45% of those 10 to 18 do. However, only 39% of people 65 and older own them, according to the Yankee Group.

Acceleration/emulation products get faster, add capacity

THE PALLADIUM II addition to Cadence's Incisive functional-verification platform is the next generation of the company's massively parallel engines. It uses high-speed on-chip memory, high-bandwidth interconnect, and multichip-packaging

technology. This architecture allows direct communication between every processor in a Palladium system and supports a bandwidth of 190 MHz. It supports compilation of as many as 30 million gates per hour and a runtime performance of 1 MHz.

The system allows you to

connect as many as 61,440 I/O signals to verify a full system or multiple chips in parallel. In addition, the multiuser mode can support as many as 32 users independently running both in-circuit emulation and simulation acceleration. Users can access the system from different sites and

verify multiple pieces of their hardware and software code.

The advanced verification environment in the new system provides comprehensive support for hardware/software verification. Capabilities now include transaction-based acceleration, verification IP (intellectual property), integration with software debuggers, assertion-based acceleration, support for all the languages in the Incisive platform, and support of the Linux operating system. Cadence also offers the new system through its Acceleration-on-Demand program, whereby users can swap Incisive Uni-

fied Simulator licenses for additional accelerator or emulator capacity at runtime. Price of a basic configuration, including nine Incisive-simulation swappable licenses and a capacity of 3.6 million gates, is \$380,160 for a time-based license.—by Gabe Moretti

► **Cadence**, 1-408-943-1234, www.cadence.com.

RF DESIGNERS GET MICROWAVE SUPPORT

Applied Wave Research's Microwave Office 2004 design suite for RF- and microwave-design engineers integrates 3-D planar electromagnetic simulation with circuit-simulation and -layout tools. The EM simulator, which uses a full-wave spectral-domain approach, handles designs as much as five times larger than the previous version. The tool also provides a dynamic EM-extraction capability that lets designers select and target schematic elements for simulation using any of the EM-socket-interface solvers. The tool includes improvements in harmonic-balance simulation, layout, and GUI, and it adds new models. Microwave Office 2004 runs under Windows NT4, 2000, XP, and Linux. Prices for a yearly, time-based license range from \$8000 to \$40,000, depending on the configuration.

—by Gabe Moretti

► **Applied Wave Research**, 1-310-726-3000, www.mwoffice.com.

Programmable logic aims for automotive apps, proliferates low-price spins

AUTOMOTIVE-ELECTRONICS applications are now sufficiently alluring, according to Xilinx, to justify dedicated-testing device variants, and the XA product spins are the result. Both Q-grade options, which operate at -40 to +125°C, and I-grade options, which operate at -40 to +100°C, are available with four device families: the 1.8V Spartan-IIE and 1.2V Spartan-3 FPGAs, along with companion configuration-flash memories, and 3.3V 9500XL and 1.8V CoolRunner-II CPLDs. The XA line supports the AEC-Q100 qualification flow, ISO-TS16949 certification, the PPAP (Production Part Approval Process) and managed PCNs (product-change notices), and extended product-life cycles.

All products are now available in sample quantities; Spartan-IIE devices are scheduled to enter volume production in the first quarter of next year, flash memories and all Spartan-3 proliferations will go into pro-

duction one quarter later, and CPLDs will follow in the third quarter. The XA3S50, when in production, will cost less than \$4.50 (25,000), and the XA2C32A will cost less than \$1.25.

Xilinx has also broadened its EasyPath cost-reduction program to embrace its Spartan-3 and Virtex-4 FPGA families (see "Silicon segmentation," *EDN*, Sept 18, 2003, pg 57). Whereas Xilinx has claimed that its EasyPath devices are comparable in cost with gate-array and structured ASICs, the company has ratcheted up its bravado, now claiming that its prices are not only 30 to 80% less than full-featured FPGA counterparts, but also less than the structured-ASIC alternative. Judge for yourself: The Spartan-3 EasyPath E3S1500, for example, will sell for \$12.95 (50,000) with \$75,000 nonrecurring-engineering charges in the second half of 2005.—by Brian Dipert

► **Xilinx**, 1-408-559-7778, www.xilinx.com.

► **According to the UN Economic Commission, 607,000 automated domestic helpers were in use by the end of 2003. Most of them—570,000—were vacuum cleaners.**

PC/104 cards target analog applications

OCTAGON SYSTEMS has recently expanded its PC/104 line with four analog cards for industry, transportation, commercial-off-the-shelf-military, and medical applications. The cards include analog-I/O, digital-I/O, and timing functions. One of the cards, the DMM-32-AT, offers 32 analog inputs with 16-bit resolution, a 200k-sample/sec maximum sampling rate, and a programmable input range. In addition, the board features four analog outputs with 12-bit resolution; 31 lines of digital I/O; and a general-purpose, 16-bit count-

er/timer. An output-only module, the RMM-1612, provides 16 channels of 12-bit-resolution analog output on a single PC/104 module.

All modules in the family provide autocalibration under software control, making the data stable over the temperature range. The use of digital zero and span adjustments eliminates shifts due to vibration and temperature. All modules also contain dc/dc converters to provide low-noise power to the analog circuitry and allow 5V-only operation. The cards operate from -40 to $+85^{\circ}\text{C}$ or -20 to $+70^{\circ}\text{C}$. Prices range from

\$345 to \$595 (small quantities), including software drivers.—by Warren Webb

►**Octagon Systems**, 1-303-430-1500, www.octagon-systems.com.



New analog PC/104 cards feature high-resolution ADC, DAC, and timing functions with software autocalibration.

Chip sets revisit AMD prospects

THE LAST TIME THAT ATI Technologies rolled out AMD-targeted core-logic chip sets, AMD was a far less formidable presence in the x86 microprocessor market than it is today (see “Embedded graphics goes with the trends,” *EDN*, April 4, 2002, pg 22). As a result, ATI’s Radeon 320 IGP companion chips for AMD desktop PCs never entered volume production. ATI concentrated its AMD efforts on mobile-PC opportunities, and the company focused *most* of its development energy on Intel CPU-based alternative designs employing the 330 and 340 IGP chip sets, along with follow-on Radeon 7000 and 9100 IGP devices.

Fast-forward two and a half years, and the situation is far different: AMD’s Athlon-64 and Sempron CPUs have been tremendously successful, whereas Intel has experienced several high-visibility stumbles, the latest of which is the cancellation of the 4-GHz Pentium 4. As a result, ATI is revisiting the AMD market, and the Radeon Xpress 200 series of chip sets is the outcome of this re-engagement.

The 200G proliferation of the north-bridge chip includes a 300-MHz Radeon X300-derived graphics core that processes two pixels per clock and can run either with a dedicated frame buffer or in UMA (unified-memory-architecture) mode, an approach that is especially challenging

with AMD’s CPUs’ integrated DRAM controllers. The pinout-compatible 200P strips out the integrated graphics; both north-bridge proliferations optionally connect to a separate graphics board over a 16-lane PCI Express interface and contain four $\times 1$ PCI Express buses for Gigabit Ethernet and other high-performance interconnect applications.

ATI historically used the 66-MHz, 32-bit, proprietary, PCI-derivative A-Link north-to-south-bridge interconnection in its chip sets. With Xpress 200, conversely, ATI has embraced industry-standard dual-lane PCI Express. The south-bridge chip common to both the 200G and 200P supports four SATA ports with RAID 0 and 1 capability and two PATA ports, eight USB 2.0 links and legacy PCI connections, and AC’97 capability. (It does not yet support high-definition audio.) The production-ready Radeon Xpress 200 family’s flexibility translates to system designs at a range of predicted prices—from less than \$700 to several thousand dollars. A mobile spin of Xpress 200 is on the way, along with Intel-CPU-tuned desktop and mobile variants of the architecture, which should debut early next year.—by Brian Dipert

►**ATI Technologies**, 1-905-882-2600, www.ati.com.

►**The total market for digital-satellite set-top boxes will reach 71 million in 2008, forecasts InStat/MDR.**

Protocol modules simplify embedded networking

ELIMINATING ONE of the most complex portions of a networked design, FieldServer Technologies recently announced a quick and easy method of adding serial and Ethernet protocols to embedded controllers. The company's family of ProtoCessor modules delivers plug-in connectivity to all the common communications protocols for building automation,

process control, remote-site monitoring, utility automation, transportation, and materials handling. "While a typical embedded controller may be implemented with a \$5 microcontroller, some communications protocols need a 32-bit processor and 8 Mbytes of RAM," says Edward Hague, chief technology officer.

Typical ProtoCessors include the Industrial Ethernet

Protocol (Ethernet/IP), BACnet (Building Automation and Control) network, Metasys building-management protocol, SNMP (Simple Network Management System), and DNP (Distributed Network Protocol). Future protocols include LonWorks and ZigBee. The appropriate testing laboratories certify ProtoCessors for the protocols they support and eliminate the need to maintain in-house protocol support services.

Prices for ProtoCessor begin at \$250 (100). An RDK (rapid-development kit) is also available and includes application source code in C, a compiler, two ProtoCessor modules, debugging tools, test tools, documentation, and technical support. The RDK sells for \$1995.

—by Warren Webb

► **FieldServer Technologies**, 1-408-262-2299, www.fieldserver.com.



The ProtoCessor standardized interface allows designers to ensure compatibility with a broad range of serial and Ethernet-protocol requirements.



IN MEMORY OF BILL TRAVIS

We are sad to announce the death of Bill Travis, a long-time technical editor at *EDN*, an industry veteran, and our Design Ideas guru. He had a strong sense of good writing and proper English, and he was an expert at detecting and denouncing hype and hot air. He was a great cook, an avid pool player, and a big fan of spicy food. No slave to political correctness, Bill had a fierce and sharp sense of humor.

We will miss him.

Microcontroller targets portable-system applications

OKI SEMICONDUCTOR'S ML69Q6200/500 microcontroller series integrates a 32-bit ARM946E core with a high-speed USB2.0-device controller with an on-chip MAC (media-access-controller)/PHY (physical layer); an Ultra-DMA66 ATA interface; and flash, SRAM, and SDRAM external interfaces. Available middleware for the devices includes USB mass-storage drivers and a FAT (file-allocation-table) 16/32-bit file system that target these devices at portable-hard-drive-based applications. The 6500 series devices also include a 16-bit audio codec with a maximum 48-kHz sampling rate; a microphone preamp and headphone amplifier; and middleware for audio, such as MP3 encoding and decoding, SRS WOW, and tempo control. The ARM946E core includes a 32-bit ALU, a barrel shifter, and an enhanced 32-bit MAC block.

These devices operate as fast as 120 MHz and offer low

power consumption tuned for portable-audio applications using hard-disk drives. They include an 8-kbyte instruction and data cache; 128 kbytes of SRAM; 16 kbytes of boot ROM; as much as 512 kbytes of flash ROM; an I²S transmitter interface; a 16-bit PWM; and a four-channel, 10-bit ADC. The ARM RealView development tools support software development for these devices. The company plans next year to offer an Oki version of the ARM9 development tools, similar to the Oki ARM7 development tools. These devices are available for sampling. The 6200 series devices sell for \$9 to \$10 (100,000) with on-chip memory options ranging to 512 kbytes of flash. The 6500 series devices are available with optional licensing for the middleware; pricing is based on 1 million units.

—by Robert Cravotta

► **Oki Semiconductor**, 1-408-720-1900, www.okisemi.com.

► **Japan, home to 800,000 industrial robots, is the most robotized economy.**

Structured-array product line stalks FPGA progress

XPRESSARRAY-II IS AMI Semiconductor's newest structured-ASIC silicon product. The company intends it for FPGA conversion of programmable-logic designs that have moved to higher volume production. Target families are complex programmable parts, such as Altera's Stratix and Xilinx Virtex-II and II Pro. XPA-II parts are fabricated in standard prefabricated wafers at TSMC, in 0.15-micron CMOS, and are configured by final metallisation for interconnect at AMI's own facility. AMI describes the conversion process as low risk with low NRE (nonrecurring engineering charges), yielding a pin-for-pin compatible part with a lower per-part cost than a programmable.

XPA-II parts have 1.5V core operation, characterized down to 1.2V, with I/O operating up to 3.3V. Logic will run at up to 210 MHz and memory at up to 330 MHz (1.5V). AMI quotes power of 55 nW/MHz/gate. Reproducing some aspects of the programmables they emulate, the parts feature multistandard

I/Os with digitally controlled impedance, up to 3.4 million "ASIC gate" equivalence, and embedded DLLs and PLLs. However, AMI has chosen not to build SERDES functions onto this series, believing that designs that require on-chip SERDES are as yet at an early stage and will not be in this market space for some time; expect later parts to include these functions.

New in this series is a redistribution metal layer that allows flip-chip mounting, to handle pin counts in excess of 1000; the initial offering includes eight die sizes. AMI puts prototype turnaround at three to four weeks from acceptance of a verified netlist for an already working FPGA. The front-end design process is optimised for Synopsys synthesis tools. Expect to pay \$40 to \$240 (50,000/year) each for parts ranging from 200,000 to 500,000 equivalent gates, respectively.

—by Graham Prophet

► **AMI Semiconductor**, +32 55 33 22 11, www.amis.com.

ARM core helps licensees capture 8/32-bit-microprocessor conversions

IN 2005, ARM WILL RELEASE the IP (intellectual property) for Cortex-M3, a processor designed to take 32-bit performance into low-end applications, where silicon vendors are aiming to migrate designs directly from 8- to 32-bit microcontrollers.

A number of ARM licensees already play in this space: This core represents a more distinct segmentation of the product line to provide more cost and performance variants and to meet the trend for a number of 8-bit tasks to move to one 32-bit device. ARM states the objective for this market corner as "32-bit performance, but not at any price."

The Cortex-M3 core will be rated at 1.2 DMIPS/MHz (with a 100-MHz lowest speed when built in a TSMC 0.18-micron process). It will use 33,000 gates for the bare

core, rising to 60,000 gates for the core and its integrated system functions. ARM says the core is more than one-third smaller than any of its previous offerings. It will run applications in Thumb (including Thumb2) mode but not in the native ARM instruction set and will further reduce memory size by bit-manipulation of stored data.

It is a Harvard-architecture core, with hardware divide and single-cycle multiply. As the core will be used in event-driven applications, ARM has improved interrupt handling over ARM7; it will handle

consecutive interrupts without a separate setup/restore cycle between each. Interrupt routines can be, ARM says, written completely in C, reflecting an objective for the core to "eliminate the last vestiges of hand-crafting [of assembler]" from this sector. On chips built with the core, silicon vendors will also be able to integrate an embedded trace macrocell, which will mean improved on-chip debugging and visibility of activity during code development. The RealView tool set and others will include development support, and ThreadX, Nucleus, and OS-II—from their respective vendors—will provide RTOS support; the list will later include an OSEK environment.

Cortex-M series designs will be just one thread of a new family of products based on ARM v7 and Thumb2; there will be an A series for

complex OS-hosted tasks and an R series for deeply embedded real-time applications. ARM is also previewing the Neon core (also scheduled for 2005 release), which will add the hardware needed to support a vectorising compiler that will support media and signal-processing tasks. Silicon vendors for this core will be selling parts into applications such as streaming video and other multimedia, in wireless and high-end consumer products. It will be a 64/128-bit SIMD architecture that ARM says will coexist with the OptimoDE DSP extensions. A common thread with the low-end product is that, once again, it will remove the need for hand-optimisation of critical code segments in signal-processing applications.

—by Graham Prophet

► **ARM**, www.arm.com.

Chirped signals resist noise in 2.4-GHz band

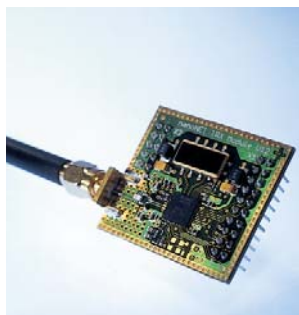
THE NANONET TRX is a transceiver for data transmission in the 2.4-GHz unlicensed band.

Designers at Nanotron have used a modulation

scheme different than most in that band, basing it on a chirped signal. The company terms it CSS (chirped spread spectrum). Chirped signals have more commonly been used in radars; a chirp (a signal burst in which the carrier frequency is continuously swept between lower and upper frequency limits) transformed by a dispersive filter is equivalent to an extremely short, high-energy pulse. In radars, it gives good distance resolution on the return echo. For data, it means that a low-level signal can achieve good data rates with very robust link performance while being resistant to a noisy environment and multipath effects.

The chip that will enter volume production early next year has a maximum data rate of 2 Mbps, achieving a range of 900m outdoors or a typical indoor range (depending on building construction) of 60m when operated at 10-mW RF output and 1 Mbps. Bandwidth per symbol is an

effective 64 MHz, and system gain using this scheme is 17 dB. For a BER (bit-error rate) of 10^{-3} , the carrier can be as much as 3 dB below the noise level. The same filter that detects the signal performs the reverse transformation on pulse interference: After passing through the filter, a pulse appears as low-level noise. At the same BER, for a 1-Mbps data rate, sensitivity is -92 dBm. The chip will run from 2.4 to 3.6V and takes 60 to 86 mA in transmit, correspon-



Nanotron's chirp-modulation data transceiver module shows the SiGe chip and the SAW filter that transforms the chirped signal.

ding to a 0.1- to 10-mW output (the level is controllable) and 40 mA in receive mode. In standby, with a real-time clock running, the chip takes 1 μ A. You will be able to evaluate the chip with the nanoNET RF module, a version of which Nanotron will introduce as a modular product. A full evaluation kit, with control processor, is also available.

The technology targets many of the same sectors as the Zigbee standard, itself based on IEEE 802.15.4: building control, telemetry, active RFID, and industrial control. But it is not necessarily competing with Zigbee, says Zigbee-alliance-member Nanotron. Rather, it could be an alternative physical layer for Zigbee for high-noise environments. The chip is built in bipolar CMOS with silicon-germanium and will initially sell for around €7.5 (100,000); modules will cost €25 (10,000). Nanotron currently implements the dispersive filter as a SAW device that adds to the bill-of-materials cost, although the company says the filter is less expensive than the chip itself. However, the company aims to replace the SAW with other filter

techniques in a later design. In its present form, the transceiver will support CSMA or TDM networking techniques.

Nanotron bases its underlying technology on MDMA (multidimensional, multiple access) with MCP (multi-choice precoding)—an echo-cancellation technique. The full implementation of these two techniques will in 2006 appear in a full-network implementation called nano-LAN.—by Graham Prophet.

► **Nanotron**, +49 30 399 9540, www.nanotron.com.

CMOS-on-sapphire makes a 1900-MHz GSM antenna switch

BETWEEN THE ANTENNA and the transmit/receive amplifiers of a cell phone, or any similar radio device, lies a switching function. It must switch the antenna between transmit and receive connections and provide a low-loss path when connected and high isolation when not. Its

function becomes more complex in a dual-, triple-, or, in the worst case, a quad-band design, when you need to connect a selection of amplifier outputs and inputs to the antenna. PIN-diode or GaAs-transistor switches have conventionally carried out this function in more complex designs. MEMS (microelectromechanical-systems)-based switches have aspired to this function but have so far failed to deliver.

San Diego-based Peregrine Semiconductor offers an alternative. Its silicon-on-insulator process—the substrate is sapphire—delivers the required performance in RF switching from CMOS transistors. With GaAs, part of the improved high-frequency performance comes from the intrinsic properties of the semiconductor and part is due to the fact that the switches are built on an insulating

substrate. Giving silicon CMOS an insulating substrate lifts its performance enough that it matches the transmit/receive switching application, according to Peregrine.

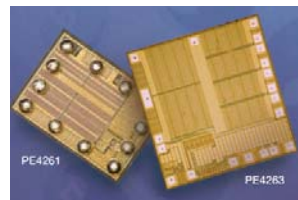
The company is offering SP4T (single-pole, four-way) and SP6T (single-pole, six-way) switches for dual- and quad-band designs, respectively. The parts come as flip-chip die for direct attachment to an RF module board; claimed benefits include an integrated CMOS decode function, no requirement for blocking capacitors (needed with pHEMT switches) or a diplexer, 1500V ESD tolerance, and direct operation from 2.6V.

The 50 Ω PE4261 (the 4T part) offers linear operation of 100 to 3000 MHz with transmitting insertion loss of

0.55 dB at 900 MHz and 0.65 dB at 1.9 GHz; isolation of 45 dB at 900 MHz and 40 dB at 1.9 GHz; low harmonics ($2f_0 = -85$ dBc and $3f_0 = -72$ dBc at 35 dBm input power); and a receiving SAW-over-voltage-protection circuit.

—by Graham Prophet

► **Peregrine Semiconductor**, +44 1923 859300, www.admiral-microwaves.co.uk (European distribution) or www.psemi.com.



CMOS-on-sapphire provides RF switching capability to compete with discrete transistors on LTCC substrates.

High-speed DSOs target the fastest serial bus signals

WITH THE INTRODUCTION of Agilent's Infini-tium DSO80000 oscilloscope, the high end of the scope business finds itself back on familiar ground, in an old-fashioned, "we've-got-more-bandwidth-than-our-competition" exchange. Agilent has raised the stakes with the 80000,

claiming 12 GHz of real-time bandwidth. (One version claims 13 GHz, but more on that below.) The instruments reach 40G samples/sec, derived by interleaving the 20G-sample/sec converters on each channel; you can run the four-channel instrument on two 40G-sample/sec channels.

Agilent sells the real-time bandwidth in 10-, 12-, and 13-GHz versions. Competitor Tektronix has recently drawn a distinction between the "native" real-time bandwidth of a scope signal path and the effective bandwidth you can claim by extending that band-

width using digital signal processing (**Reference 1**). You can effectively extend a response curve into the roll-off region by applying amplification to the whole passband, including the roll-off at the top end, and then flattening the overall response with digital filtering. Potential drawbacks include a lifting of the noise floor. Agilent acknowledges that it achieves the 13 GHz by processing the 12-GHz response, adding in passing that in previous-generation scopes, it used DSP only to flatten the response, not extend it.

The 20G-sample/sec ADC

is fundamentally the same design Agilent has used in earlier instruments. It is paired with front-end, gallium-arsenide-based amplifiers in a custom multilayer ceramic package that provides a full Faraday cage shield. Noise performance is said to be as good as the best spectrum analysers, and you can run a software package on the scope so that it becomes a vector signal analyser.

Real-time bandwidth is maintained to the probe tip by a redesign of the probe Agilent used in its previous model. Contact to the board-under-test is by small solder-in wires that bridge to a replaceable micro pc board at the probe tip. Agilent has moved the tiny resistors that were part of that wire contact in the earlier design to the probe tip itself. A high-impedance probe is essential to see the actual signal environment, Agilent says; observing at 50 Ω without affecting the signal itself is impossible. The new probe loading is 220 fF and 50 k Ω . Other innovations in the signal path include a front-panel connector that looks like, acts like, and is compatible with a BNC but is internally constructed like an N-type, with a usable bandwidth to 18 GHz.

With the response characteristics of a DSO, scope performance need not exceed measured signal characteristics by the wide margins that used to prevail. These scopes will accurately measure a 30-

psec rise time, Agilent says, and can be used on a variety of serial communications protocols with clock rates of 4 to 8 GHz. They will resolve the third harmonic of an 8-Gbps serial bus and the 5th harmonic of a 4.8-Gbps bus. As well as very low noise, the 80000 series has low intrinsic jitter (claimed trigger jitter is in the hundreds-of-femtoseconds region). Therefore, you'll see reduced error due to the instrument itself, leading to, for example, "cleaner" eye diagrams. Recognising that serial communications is likely a main area of instrument application (others include basic physics research), the instrument's software supports features such as 8b/10b decoding, and the ability to search for specific symbol sequences. With the vector-signal-analyser software, the 40-GHz input path becomes a wide-band front end, allowing the instrument to view data such as ultra-wideband signals.

Base prices for the series range from \$94,000 to \$122,000; a 12-GHz probe amplifier will cost you \$9000, and the solder-in probe head (effectively a consumable you would use a few tens of times, with care) is \$400.

—by Graham Prophet

► **Agilent**, +31 20 547 2111, www.agilent.com

REFERENCE

1. Shepard, Colin, "Evaluating oscilloscopes: Dig deeper," *EDN*, Aug 19, 2004, pg 61.



Agilent's 80000 series digital oscilloscopes take real-time bandwidths to more than 12 GHz.