

# design ideas

Edited by Bill Travis

## Software makes full use of 8051's interrupt system

Deng Yong, Shanghai Jiaotong University, China

**T**HE PROGRAM in Listing 1 uses a pseudo-RETI instruction to provide a five-priority-level interrupt system for the 8051P microcontroller. The interrupt-priority order, from high to low, is INT0 IT0 INT1 IT1 INTP. Before the pseudo-RETI instruction arrives in the IT0 or IT1 interrupt-service routine, the address of the first instruction, which is after the pseudo-RETI instruction, goes back into the stack. The internal, nonaddressable flip-flop associated with IT0 or IT1 clears to acknowledge a higher interrupt after execution of the pseudo-RETI instruction, while the IT0 or IT1 interrupt-service routine executes continuously until the RETI instruction arrives. Hardware circuits can exchange the INT1 and INT2 interrupts, and software can set the IT1 and IT2 interrupts.

You can download Listing 1 from the Web version of this article at [www.ednmag.com](http://www.ednmag.com).

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- Software makes full use of 8051's interrupt system..... 111
- Improve FET-based gain control..... 112
- Circuit improves on bias for GaAs FETs..... 114
- Build your own bypass-capacitor tester ..... 116
- DAC and op amp provide variable-control voltage..... 118
- Logic offers complementary-switch control..... 120
- Circuit measures currents in dc servo motor ..... 122

**LISTING 1—FIVE-PRIORITY-LEVEL INTERRUPT SYSTEM FOR 8051P**

```

ORG 0000H
LJMP START
ORG 0003H
LJMP INT0
ORG 000BH
LJMP IT0
ORG 0013H
LJMP INT1
ORG 001BH
LJMP IT1
ORG 0023H
LJMP INTP

START: MOV SP, #60H
      MOV IP, #0FH
      MOV IP, #03H
      SJMP $

INT0:                                     ;INT0 interrupt service program
      RETI

IT0:   RETI
      PUSH DPL
      PUSH DPH
      MOV DPTR, #True_IT0
      PUSH DPL
      PUSH DPH
      ANL IP, #1000000110B
      RETI                                     ;pseudo-RETI
True_IT0:
      POP DPH
      POP DPL
      ORL IP, #00011100B
      RETI                                     ;INT1 interrupt service program

INT1:                                     ;INT1 interrupt service program
      RETI

IT1:   RETI
      PUSH DPL
      PUSH DPH
      MOV DPTR, #True_IT1
      PUSH DPL
      PUSH DPH
      CLR PS
      RETI                                     ;pseudo-RETI
True_IT1:
      POP DPH
      POP DPL
      SETB PS
      RETI

INTP:                                     ;Serial port interrupt service program
      PUSH DPL
      PUSH DPH
      MOV DPTR, #SPINT
      PUSH DPL
      PUSH DPH
      RETI

SPINT:
      POP DPH
      POP DPL
      RETI

```

# Improve FET-based gain control

Ron Mancini, Texas Instruments, [rmancini@ti.com](mailto:rmancini@ti.com)

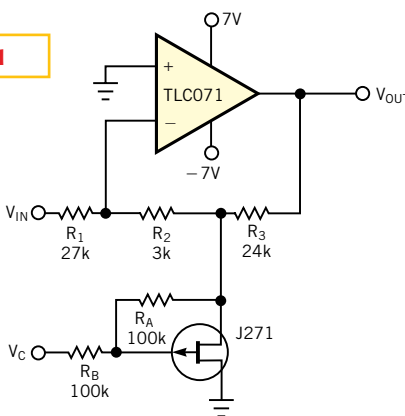
**O**NE PROBLEM with standard FET gain-control circuits is increased noise when you

use the FET as a part of a resistive attenuator in series with an op amp. This configuration attenuates the signal before amplification; hence, it requires much higher gain bandwidth and better noise performance from the op amp. When you substitute the FET for the gain-setting resistor in a noninverting op-amp circuit, distortion limits the circuit configuration to applications in which the input voltage is less than a few hundred millivolts. The FET imposes this limitation, because the channel-depletion layer is a function of  $V_{DG}$  and  $V_{GS}$ . The improved circuit in **Figure 1** uses the FET as part of the feedback loop. The voltage across the FET is limited in this application, and the noise performance is good. An added bonus is improved linearity performance. The transfer function for the improved circuit is as follows (**Reference 1**):

$$-\frac{V_{OUT}}{V_{IN}} = -G = \frac{R_2 + R_3 + \frac{R_2 R_3}{R_4}}{R_1}$$

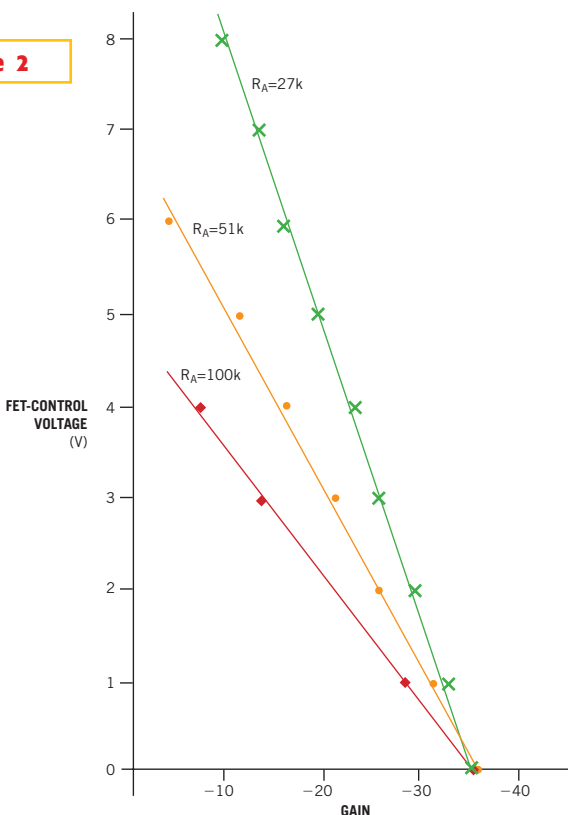
When  $R_2 + R_3 = R_1$  and  $R_4 = R_{DS}$  (FET drain-source resistance), the transfer function reduces to  $-G = 1 + R_2 || R_3 / R_{DS}$ . The minimum drain-source resistance for the FET on hand, J271, is  $76\Omega$  at  $V_{GS} = 0V$ . The actual  $V_{DS}$  at the inception of distortion varies with each FET, but keeping  $V_{DS}$  lower than 200 mV usually prevents distortion. In the design in **Figure 1**, the FET drain-source voltage is limited to approximately 100 mV to prevent distortion. The divider action be-

**Figure 1**



The drain-source resistance of the FET controls the gain of the op-amp stage.

**Figure 2**



The ratio  $R_A/R_B$  in **Figure 1** controls the slope of the gain-control transfer function.

tween  $R_3$  and  $R_{DS}$  creates  $V_{DS}$  from the output voltage, according to the following equation:

$$V_{DS} = V_{OUT} \frac{R_{DS}}{R_{DS} + R_3} = 0.1V = 5 \frac{0.076}{0.076 + R_3}$$

You can calculate  $R_3$  as 24.5 k $\Omega$  and select 24 k $\Omega$ . The parallel value of  $R_2$  and  $R_3$  determine the maximum circuit gain. Selecting  $R_2$  as 3 k $\Omega$  yields  $R_1$  equal to 27 k $\Omega$  and a maximum gain of  $-37$ . The measured gain at  $V_C = V_{GS} = 0V$  is  $-36.1$ , which correlates well with the calculated value.  $R_A$  and  $R_B$  are feedback resistors that linearize the FET's  $V_{GS}$  versus  $R_{DS}$  transfer function. You can normally obtain adequate linearization with equal-value resistors, but you can also control the slope of the transfer function by setting the resistor ratio. The graph in **Figure 2** shows that  $R_A$  modifies the transfer function and linear control-voltage range ( $V_{GS}$ ). The p-channel FET, J271, requires a positive control voltage, but you can use a negative control voltage with an equivalent n-channel FET, such as the J210. The circuit is versatile and provides low distortion, wide range, good linearity, and low cost. The TLC071 op amp has low input-bias currents and has provisions for input offset-voltage correction.

## REFERENCE

1. Mancini, Ron, "Op amps for everyone," Texas Instruments, September 2000, pg 3.

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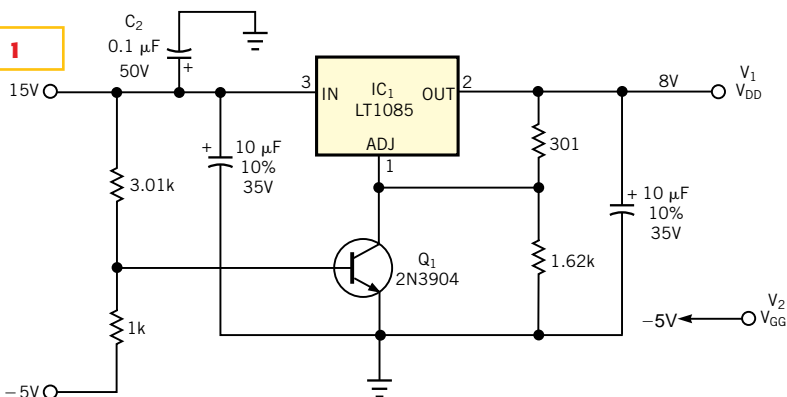
# Circuit improves on bias for GaAs FETs

Tom Roberts, Anritsu Co, Morgan Hill, CA

IT'S IMPORTANT to properly sequence the bias applied to an RF/microwave GaAs FET or a MMIC (monolithic-microwave-IC) amplifier. These devices are extremely sensitive to drain and gate voltage levels as well as to the order in which these biases turn on and off. A GaAs-FET amplifier that uses two bias voltages—a negative supply,  $V_{GG}$ , on its gate and a positive supply,  $V_{DD}$ , on its drain—requires that  $V_{GG}$  be present before the application of  $V_{DD}$ . When powering down the amplifier,  $V_{DD}$  must go to 0V before  $V_{GG}$  changes from its negative value to 0V. **Figure 1** shows a commonly used disable circuit found in many voltage-regulator data sheets. The circuit uses a 2N3904 switching transistor to pull the ADJ pin to ground to disable the voltage regulator. The circuit does not set the output of the regulator to 0V but instead sets the output to the regulator's reference voltage, 1.25V. The condition in which a GaAs FET or MMIC has 0V on the gate and 1.25V on the drain can result in damage to the device. For example, M/A-Com's MAAM26100-PI MMIC power amplifier requires 8V for  $V_{DD}$  and  $-5V$  for  $V_{GG}$ . With 1.25V on  $V_{DD}$  and 0V on  $V_{GG}$ , the MMIC draws approximately three times its nominal drain current, sufficient to cause destructive failure. **Figure 2** shows an improved circuit for the adjustable regulator.

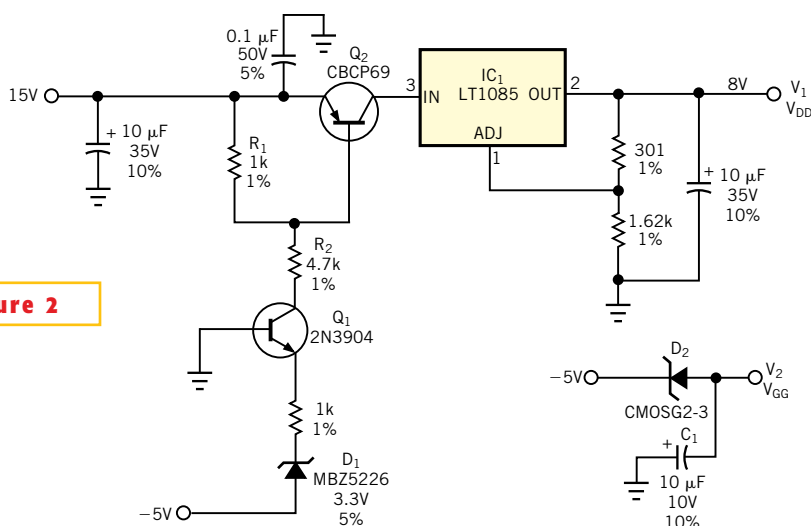
A medium-power pass transistor,  $Q_2$ , a Central Semiconductor CBCP69, connects to the input of the voltage regulator to disable the regulated output voltage. In disabled mode, the voltage at the regulator's output is 0V. In enabled mode,  $Q_1$  saturates and activates a voltage divider comprising  $R_1$  and  $R_2$ .  $Q_2$  saturates, and the output swings from 0 to 8V. Because of the propagation delay of the transistor switching network, the 8V output switches from 0 to 8V after the  $-5V$  supply switches from 0 to  $-5V$ .  $D_1$  sets the disable threshold of the  $-5V$  supply to approximately  $-4V$  to minimize the delay between the  $-5V$  supply switching

**Figure 1**



In disabled mode, this circuit supplies a potentially damaging 1.25V to the drain of a GaAs FET or a MMIC.

**Figure 2**



This circuit provides safe power-up and power-down sequencing for sensitive GaAs FETs and MMICs.

from  $-5V$  to 0V and the regulator switching from 8V to 0V. To ensure that  $V_{GG}$  remains at  $-5V$  after disabling  $IC_1$ , you can exploit the high FET gate resistance and the low-leakage Schottky-diode characteristic. The combination of high gate resistance of the GaAs FET, the low-leakage Schottky diode,  $D_2$ , and the 10-μF capacitor,  $C_1$ , provides a high  $V_{GG}$  RC time constant when the  $-5V$  supply is off

(in other words, at 0V). The RC time constant of the Schottky-diode leakage resistance, the FET gate resistance, and  $C_1$  is long compared with the RC time constant at  $V_{DD}$ . As well as having low reverse leakage,  $D_2$  has an inherently low (0.1V) forward drop.

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# Build your own bypass-capacitor tester

Carl Pugh, Pugh Magnetics, Newark, CA

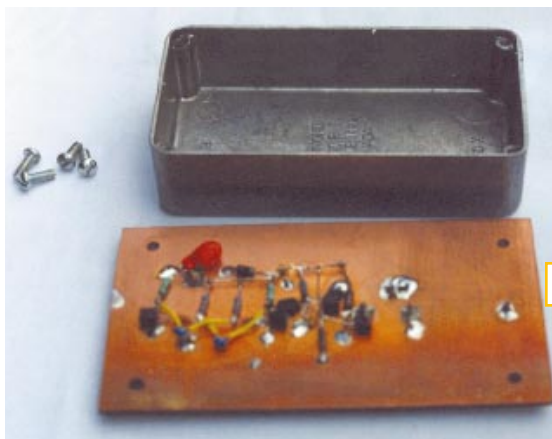
**M**OST CIRCUITS USE bypass capacitors and can deliver substandard performance if the capacitors have poor pulse characteristics. Few if any articles cover how to test bypass capacitors for pulse characteristics. The circuit in **Figure 1** tests these characteristics. It charges the capacitor under test through 100 k $\Omega$  for approximately 1 msec and then discharges it through 10 $\Omega$  for approximately 40 nsec. The cycle then repeats. The circuit uses a double-sided copper-clad pc board. All the components except the 10 $\Omega$  resistor connect to one side of the board, so they can benefit from shielding by the cast-aluminum enclosure (**Figure 2**). All leads are as short as possible and as close as possible to the copper-clad board. The layout is such that you don't need the oscilloscope probe's ground lead; the ground on the probe contacts a ground post on the pc board. The ground posts, feedthroughs, connections to the capacitor under test, and oscilloscope probes use vector-board terminals.

The circuit comprises an astable multivibrator using two 2N3904 transistors,

Q<sub>1</sub> and Q<sub>2</sub>, and associated components. A voltage reducer/shaper uses a trimmer capacitor, C<sub>1</sub>; a 100-pF capacitor, C<sub>2</sub>; and a 200 $\Omega$  resistor, R<sub>1</sub>. An amplifier uses a 2N3906 transistor, Q<sub>3</sub>, and associated components, and a power amplifier uses a PN2222A transistor, Q<sub>4</sub>, and associated components. C<sub>1</sub>, C<sub>2</sub>, and R<sub>1</sub> produce a fast rise- and fall-time, 0.7V pulse when the multivibrator's output switches negative. Because the Q<sub>3</sub> transistor has no bias, it conducts only at the peak of the

input pulse and produces a pulse with fast rise and fall times. The output from the Q<sub>3</sub> drives Q<sub>4</sub>, causing that transistor to conduct for approximately 40 nsec. You can obtain interesting results when testing capacitors with long leads and then testing the same capacitors with short leads, corroborating the universal advice to keep leads short.

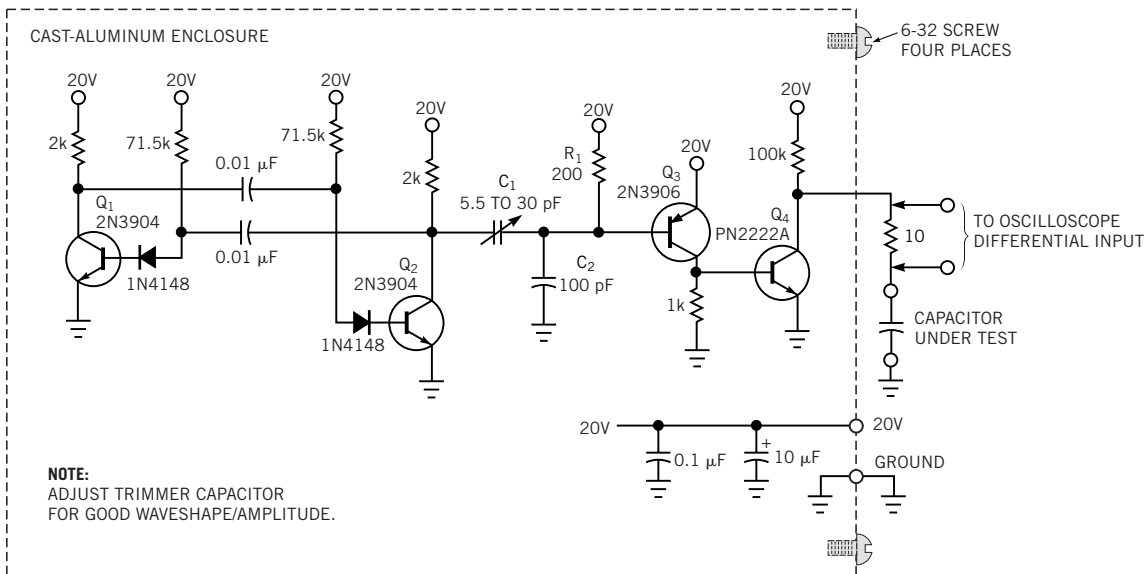
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**Figure 2**

Components all connect to one side of the pc board, and a cast-aluminum cover provides shielding.

**Figure 1**



Test the pulse characteristics of bypass capacitors using this simple circuit.



containing standard R-2R ladders, this approach offers lower supply voltages, higher speed, and smaller packages. The DAC, IC<sub>3</sub>, operating with a 2.5V reference voltage from IC<sub>1</sub> and driven by microcontroller IC<sub>2</sub>, produces an output swing

from 0 to 2.5V. Op amp IC<sub>4</sub> inverts and amplifies this output to produce a 0 to -5V output. For test purposes, the software routine in **Listing 1** commands the microcontroller to generate a 0 to -5V triangle-wave output. You can download

the listing from the Web version of this article at [www.ednmag.com](http://www.ednmag.com).

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## Logic offers complementary-switch control

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**T**HE COMPLEMENTARY-SWITCH controller in **Figure 1** uses a few inverters to provide drive signals for the complementary switches. Complementary-switch configurations find widespread use in synchronous-rectification circuits, charge pumps, full-bridge control circuits, and other circuits. The circuit in **Figure 1** provides not only a complementary drive signal but also a deadtime delay on both rising and falling edges. The high-speed inverter gates use IC<sub>1</sub>, a 74HC04 CMOS circuit, and 1N5819 Schottky diodes D<sub>1</sub> and D<sub>2</sub>. The 74HC04 inverter features symmetrical input thresholds, V<sub>IHM</sub> and V<sub>ILM</sub>, at 70 and 30% of the supply voltage, respectively. In **Figure 1**, IC<sub>1A</sub> inverts the signal at Node A to produce  $\bar{A}$ . When  $\bar{A}$  rises, C<sub>1</sub> rapidly charges through D<sub>1</sub>. Output B drops immediately because of IC<sub>1B</sub>'s inversion. However, Output C drops after a delay time that R<sub>2</sub> and C<sub>2</sub> determine because D<sub>2</sub> is reverse-biased. The following formula gives the delay time, t<sub>1</sub> (**Figure 2**):

$$t_1 = -R_2 C_2 \ln \frac{0.7 V_{DD}}{V_{DD}} = -R_2 C_2 \ln 0.7.$$

When  $\bar{A}$  falls, C<sub>1</sub> discharges through R<sub>1</sub>. Output B rises after a delay time that R<sub>1</sub> and C<sub>1</sub> determine. C<sub>2</sub> discharges rapidly through D<sub>2</sub>, and output C rises immediately. The following formula gives the delay time, t<sub>2</sub>:

$$t_2 = -R_1 C_1 \ln \frac{V_{DD} - 0.3 V_{DD}}{V_{DD}} = -R_1 C_1 \ln 0.7.$$

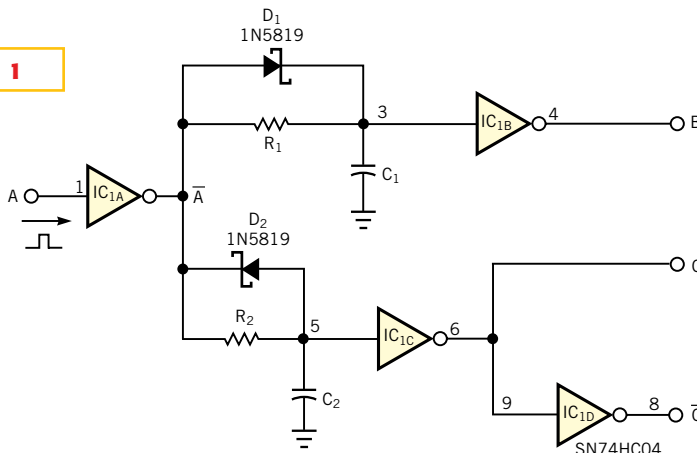
By inverting C, IC<sub>1D</sub> can provide  $\bar{C}$  a signal with the same polarity as B. By selecting values for R<sub>1</sub>, C<sub>1</sub>, R<sub>2</sub>, and C<sub>2</sub>, you

can program the delay times. The delay can be as short as 50 nsec and as long as several milliseconds. This range provides flexible, optimized control for target devices. R<sub>1</sub> and R<sub>2</sub> should be larger than 2

kΩ because of the limited current available from the inverter IC.

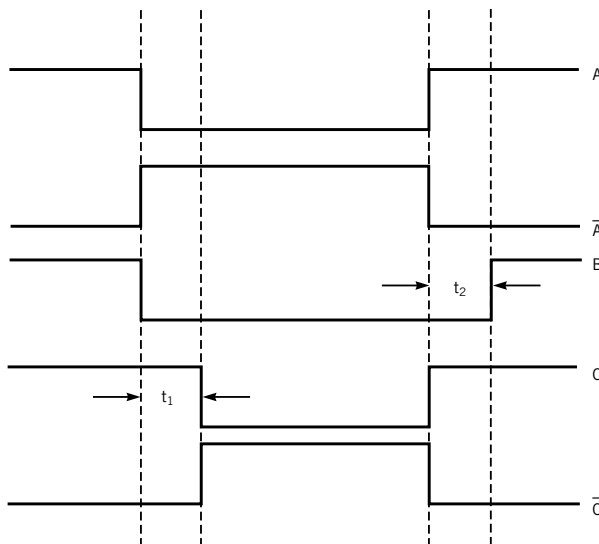
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**Figure 1**



This circuit provides drive for complementary switches with programmable deadtimes.

**Figure 2**



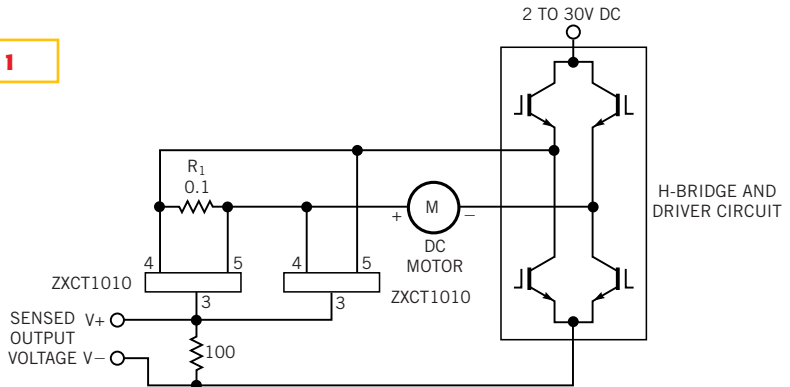
By manipulating the resistor and capacitor values in **Figure 1**, you can program t<sub>1</sub> and t<sub>2</sub>.

# Circuit measures currents in dc servo motor

Shyam Tiwari, Sensors Technology Private Ltd, Gwalior, India

**T**HE SIMPLE CIRCUIT DESIGN in **Figure 1** lets you measure all components of a current flowing in a dc servo motor. The rectified output of the circuit uses ground as a reference, so you can measure the output by using a single-ended A/D converter. The current-sense resistor,  $R_1$ , has a value of  $0.1\Omega$ . The Zetex (www.zetex.com) ZXCT1010 IC converts the differential signal across  $R_1$  to a single-ended signal. Two of these ICs form a signal rectifier. The single-ended signal makes measurement by an A/D converter cost-effective, small, and frugal in power consumption. The method also makes it possible to measure current from many sources at a time, such as in robots that use multiple servo motors. Measurement accuracy is approximately  $\pm 3\%$ , which is adequate in most dynamic systems. Hence, an 8-

**Figure 1**



With this simple circuit, you can measure the currents in a dc servo motor.

bit A/D converter suffices to digitize the signal. If an average value of the current is of interest, then you can place an averaging capacitor between the  $V+$  and  $V-$  terminals to remove the ac compo-

nent. The unfiltered signal has 300-kHz response to ac current.

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