



leading edge

What's hot
in the
design
community

Edited by
Fran Granville

And thou beside me...with thy wallet
"A loaf of bread, a jug of wine, and thousands of other consumer items: Sooner or later, inflation will hit all of them. In one funny little corner of the economic universe, however, that law doesn't apply. It's consumer technology, where prices head ever downward even as power and features improve."

—David Pogue,
in *The New York Times*,
Nov 20, 2003

Fan card boosts embedded reliability

By Warren Webb

A NEW PC/104 MULTIFUNCTION module from Parvus provides embedded systems with temperature-controlled, forced-air cooling along with environmental monitoring of humidity and pressure

conditions. The ThermoCool Environmental Fan Card II includes two high-efficiency, brushless fans that turn on and off in response to changing temperature while conserving power and increasing product life. In a sealed enclosure, the device can effectively reduce or even eliminate the need for an embedded system for outside air exchange. The card drives air in a push-pull, circular cooling pattern around the fan module and adjacent PC/104 cards.

The Environmental Fan

Card II also integrates capaci-

ty-humidity and atmospheric-pressure sensors, which you can use as alarm indicators. Other standard features include two Form C relays, two digital inputs, multiple analog inputs, and Windows 9x, NT, 2000, and XP drivers. Prices start at \$187 (100).

► **Parvus Corp**, 1-801-483-1533, www.parvus.com.



The ThermoCool Environmental Fan Card II offers temperature-controlled cooling plus humidity and pressure monitoring for PC/104 systems.

Synthesizable cores target low power

THE SC1200 AND SC1400 DSP cores are the first members of Starcore's synthesizable SC1000-family of 16-bit DSP cores. The SC1200 core is a two-MAC (multiple-accumulate), four-issue VLES (variable-length-execution-set) architecture that targets power-efficient applications for portable devices. The SC1400 targets data-intensive applications with four MACs and a six-issue VLES architecture. These cores are fully synthesizable and can target any wafer-fab process variation, including ultra low-leakage processes. Metrowerks (www.metrowerks.com) and Green Hills (www.ghs.com) provide software-development tools for these cores and include support for RTXC, OSE, SmartDSP, and ThreadX operating systems.

The two cores are each available as stand-alone cores or as part of three preintegrated platforms. The primary platform

comprises one of the SC1000-family DSP cores and an on-chip emulator that can support real-time debugging through a JTAG interface. The embedded platform adds an AHB (Advanced High-Performance Bus) 2.0-compliant bus master, a 120-level, triggered interrupt-control unit, gated control for dynamic power reduction, and a configurable memory controller that can support an attachable DMA controller. The advanced platform adds a mapped accelerator-interface unit that enables you to attach accelerators and other custom memory-mapped hardware to the core, and it expands the memory-controller subsystem with program- and data-cache controllers. All of these platforms are available for immediate licensing ranging from single projects to ASIC licenses.

—by Robert Cravotta

► **Starcore**, 1-512-682-8500, www.starcore-dsp.com.

Upgrade backplanes to 10 Gbps with 0% coding overhead

TRANSFERRING PAYLOADS as fast as 10 Gbps per differential pair with 0% coding overhead, the AN6420 quad high-speed backplane SERDES (serializer/deserializer) transceiver from Accelerant

Networks operates at 6.25 to 10 Gbps using PAM4 (pass-band-amplitude-modulation) multilevel signaling. The device also interoperates with SERDES devices that operate as fast as 5 Gbps with DFE (decision-feedback equalization) in binary mode. You can use DFE to open eyes as small as 5 mV to guarantee signal integrity.

Coding schemes, such as 8B/10B or turbo coding, traditionally improve the robustness of a link by providing an error-correction mechanism—usually, an embedded pattern—within the raw bandwidth of the link, which may enable limited repair of corrupted data, thus increasing the BER (bit-error rate). Additionally, coding guarantees a certain transition density, giving the data enough transitions for the receiver clock to lock onto the signal. Coding thus improves the ef-

fective BER of a link; for example, with turbo coding, a link with a BER of 10^{10} might increase to 10^{18} but at the cost of as much as 25% of the available bandwidth.

The AN6420 adds 0% coding overhead by achieving a BER of 10^{18} through other means, eliminating the need for coding and the associated loss of bandwidth. The transmitter includes a random polynomial scrambler, which guarantees transition density and uses a lossless-compression scheme to account for extreme-transition cases without increasing the payload. A distributed-digital-PLL architecture retimes signals traveling from one side of the chip to the other to keep jitter less than 2 psec rms. Ad-

ditionally, Accelerant's "lab-in-a-chip" technology has undersampling, margining-algorithm, and vector-analyzing diagnostic units to produce an in situ BER to track link reliability on a per-link basis. You can access BER data via registers and analyze it using a company-provided GUI, which Accelerant based on the Mathworks' (www.mathworks.com) MatLab.

Because the effective overhead is 0%, you can use the

coding overhead. For example, instead of requiring 6.25 Gbps to pass a 5-Gbps XAUI (10-Gbit attachment-unit-interface) data stream, the AN6420 can operate at 5 Gbps. Running at a lower frequency reduces overall power consumption and enhances the range of backplanes over which the device can reliably operate.

In addition to operating as far as 60 in. over FR4, the AN6420 supports both transmitting and receiving equalization, has continuously adaptive seven-tap transmitter equalization, loss-of-signal detection, programmable per-channel BER tester, ± 400 -ppm frequency offset, and the ability to receive and transmit asynchronously. The device also has a quad 2-to-1 backplane multiplexer, allowing such functions as the multiplexing of two 3.125-Gbps



The AN6420 quad backplane transceiver consumes 0.2W per 10-Gbps channel across 20 in. of FR4 and two backplane connectors with a maximum range of 60 in., all with 0% effective overhead.

entire bandwidth to pass data; in typical 8B/10B encoding, 25% of the bandwidth is en-

XAUI channels onto a single 6.25-Gbps channel. The AN6420 consumes 0.2W of power per 10-Gbps channel across 20 in. of FR4 and two backplane connectors.

Currently available for sampling, the AN6420 uses a 0.13-micron process, and the company plans to build a later version on a 90-nm process. It comes in a 17x17-mm, plastic BGA package and costs \$80 per unit (volume quantities).—by Nicholas Cravotta

► **Accelerant Networks**, 1-503-466-9231, www.accelerant.net.

DILBERT *By Scott Adams*



► **Global semiconductor sales increased to \$14.4 billion in September 2003 from \$12.3 billion in September 2002, the Semiconductor Industry Association said in a statement on its Web site. The growth marked the seventh consecutive monthly gain. Sales rose 6.5% from August.**

System processor paces DVD-player cost reduction, feature-augmentation trends

DVD-PLAYER PRICES HAVE TUMBLED to less-than-\$50 retail levels, and full-featured units with progressive-scan video outputs and compatibility with both DVD-Audio and SACD (Super Audio CD), high-resolution audio formats recently broke through the \$200 barrier (see

“Upward spiral,” *EDN*, Aug 7, 2003, pg 38). System manufacturers, challenged to reduce bill-of-materials costs, consequently pressure their chip suppliers to remove dollars and cents from the platform budget. And chip suppliers predictably turn to the integration capability of advanced deep-submicron-manufacturing processes to combine multiple chips’ functions into one, addressing customers’ price expectations and still turning a profit.

LSI Logic’s ZiVA-6 processor family—priced at as much

as \$10 (1 million)—builds on the previous-generation ZiVA-5 by including a modular pick-and-choose plethora of added features: an S/PDIF (Sony/Philips digital interface) receiver, a hardware SACD decoder and PCM transcoder, a PCMCIA controller, front-end servo logic, and dual-channel audio DACs. Note that, to implement a DVD player with six-channel analog output, you still need to add external DACs. Copy-protected HDMI (high-definition-multimedia interface) and IEEE-1394 digital outputs for

audio and video also require separate silicon. The PCMCIA interface, suitable for hookup to removable memory cards containing photos and other data, also delivers sufficient bandwidth for a wireless IEEE-802.11b module. Higher speed 802.11a and 802.11g connections might, depending on protocol and system overhead, require a faster CardBus port.

The company bundles a low-end ZiVA-6 with a loader and motor driver, along with relevant documentation and software, to come up with the ready-for-production ZiVA-6MK reference design, which offers a less-than-\$30 estimated bill-of-materials cost. Samples of the ZiVA-6 processor family will be available by the end of this quarter, LSI Logic claims. The company has scheduled production for early next year.—by Brian Dipert
▶**LSI Logic**, 1-408-954-3108, www.lsillogic.com.

RF transceiver tackles 2.4-GHz ISM band

The latest RF entry from Chipcom AS extends its family of RF transceivers past the 1-GHz line in the ether into the 2.4-GHz unlicensed ISM (industrial, scientific, and medical) band. The CC2400 IC meets European, Japanese, and US regulations and provides data rates as high as 1 Mbps. The device targets use in point-to-point links, such as game controllers, wireless-audio headsets, and leisure equipment. It uses direct-I/Q upconversion for continuous transmissions without a limit on packet length, an attribute that some headset and audio applications require.

You can select data rates as low as 10 kbps if you don’t need the highest rate but do wish to reduce power dissipation. Range is up to 100m at the lowest data rate. The CC2400 is well-suited for frequency-hopping spread-spectrum and multichannel systems, such as game controllers with four simultaneous users. It sells for \$2.40 (100,000) and is available with a PC-based/USB-port development kit, which includes a pair of motherboards and radio modules for a full-duplex development environment.—by Bill Schweber

▶**Chipcom AS**, www.chipcom.com.

YES, WE DO HAVE BANANAS

Banana jacks, that is. Hard to believe, but, even in this day of supersmall connectors and RF interconnections, basic test, medical, and industrial applications still use the venerable banana-style jack and mating-plug pair.

Safety banana jacks from



These safety banana jacks from Cal Test Electronics are available in two body styles, eight wire-attachment styles, and 10 colors.

Cal Test Electronics are available in threaded-body/panel-nut as well as push-in-body styles with a choice of eight wire-attachment methods and 10 colors.

These jacks meet all established safety standards to protect the user from hazardous live voltage, including an insulating sheath for the contact spring of the mating plug. Prices begin at 75 cents.

—by Bill Schweber

▶**Cal Test Electronics**, 1-888-256-2246, www.caltestelectronics.com.

▶**PCs, which are 30% of the end market for semiconductors, had a third-quarter 2003 increase of 33% in DRAM chips and a 24% increase in microprocessors, according to the Semiconductor Industry Association.**

IP supports High-Speed USB host controllers

ARC HAS ANNOUNCED two USB-host-controller IP (intellectual-property) offerings, the USB-HS SPH (single-port-host) and the USB-HS MPH (multiport-host) cores. The SPH core's latency-based

architecture sports the lowest gate count for a single-port, high-speed host controller and supports USB low-, full-, and high-speed (to 480-Mbps) data bandwidths. The core includes a functional subset of the HS-OTG (On the Go) IP core, is EHCI (Enhanced Host Controller Interface)-compatible, and supports UTMI (USB 2.0 Transceiver Macrocell Interface) and ULPI (Unit Level Prototype Implementation) PHYs (physical-layer interfaces). The USB host-specific controllers support programma-

ble features, such as adaptive tuning, programmable fill level, and enhanced streaming, under software control.

The MPH IP core is a superset of the SPH product supporting two to eight controller ports. Each controller port is backward-compatible and can operate individually at high, full, or low speed. The integrated transaction translator enables a combined bandwidth of 480 Mbytes/sec for the high-speed ports to share and a combined bandwidth of 12 Mbytes/sec for the full-speed ports to share.

The SPH and MPH High-Speed USB cores are available as synthesizable, technology-independent VHDL or Verilog RTL source code, and they include simulation testbenches, synthesis scripts, USB software stacks, and class and device drivers. ARC offers PHYs and PHY macrocells that in-

teroperate with the USB controllers through ARC's CERTIFY program. The USB-HS SPH controller is now available for licensing. The USB-HS MPH controller will be available in fourth quarter of this year.

—by Robert Cravotta
►ARC, www.arc.com.

MOSFETs push figure of merit to 60% below existing value

A SET OF FOUR MOSFETs from Vishay Siliconix pushes the traditional figure of merit—on-resistance time and gate-drain capacitance—to new lows. The lower on-resistance translates to improved efficiency and less heat in a smaller package; the lower gate-drain capacitance improves switching performance at high frequencies. Targeting 20A (Si4390DY and Si7390DP) and 40A (Si4392DY and Si7392DP) output-current designs, these MOSFETs are available in various SO-8 package versions.

Drain- and gate-to-source voltages are 30 and 20V, respectively; on-resistance is approximately 10 mΩ at 4.5V and 13.5 to 16.5 mΩ at 4.5V. Gate-drain capacitance is 10 nC at 4.5V; the figure of merit at that voltage is 135 to 165, depending on model and packaging. These MOSFETs sell for 55 cents each (100,000).

—by Bill Schweber

►Vishay Siliconix, www.vishay.com.

Book provides practical tips on high-speed pc-board design

WHEN DEVELOPING DESIGNS, engineers often face problems they have not previously encountered. Unless you know someone who has successfully solved the problem, you must research the literature for a theoretical hint to the solution or find a solution by trial and error. Both alternatives are time-consuming and error-prone. Now, Lee W Ritchey has written a book that addresses this issue, using his considerable experience in designing high-speed circuits. *Right the First Time: A Practical Handbook on High Speed PCB and System Design, Volume One* presents practical solutions to most of the problems facing developers of high-speed pc-board products.

The author calls this book *Volume One* because, when he was halfway through writing it, he realized that much more remains to discuss about this topic. Yet, he did not want to either delay the publication or complicate the contents by cramming every hint, solution, and illustration into one book. The book attempts to help electrical and electronics engineers, including pc-board designers, to develop correctly functioning boards without rework. It draws on more than three decades' worth of Ritchey's experience in virtual prototyping of high-speed pc boards in all types of products. It discusses all of the steps in the process—from selecting tools to selecting suppliers. It also includes many figures—from schematics to oscilloscope graphs and logic-analyzer outputs—to help you visualize both the problem and the solution.

The 230-pg text also includes a glossary; an extensive bibliography; and appendixes that cover related subjects, such as the description of a plated through hole, how to select a pc-board supplier, and conversion tables. The book sells for \$125, and you can order it from the author's Speeding Edge Web site.—by Gabe Moretti
►Speeding Edge, 1-707-568-3983, www.speedingedge.com.

►The market for semiconductors in flash memory and DSPs rose 27 and 20%, respectively, in the third quarter of 2003, according to the Semiconductor Industry Association. The increases were driven by cell phones, which account for 12% of semiconductor use.

Hybrid controllers extend performance and integration

THE NEW 56F8300 SERIES hybrid controllers from Motorola extend the performance and integration options for 16-bit automotive and industrial applications. The company based the six

new devices on the 56800/56800E hybrid core. They integrate a 60-MHz controller and signal-processing core with 32- to 256-kbyte flash program memory with a flash security feature, a FlexCAN

(controller-area-network) module, and as many as 76 general-purpose I/O ports. The third-generation flash on these devices operates as fast as 60 MIPS without using acceleration technology. The in-

tegrated controller-level, safety-focused functions include a temperature sensor, multiple fault conditions, built-in write-protection registers, and on-chip clock synthesis that allows graceful shutdown to prevent system damage.

The first six devices in the 56F8300 family are currently available for sampling for prototyping with prices ranging from \$8.13 (10,000) for the 32-kbyte flash MC56F8322 to \$15.93 (10,000) for the 256-

kbyte flash MC56F8357 devices.

The devices are available for extended-temperature ranges of -40 to $+125^{\circ}\text{C}$. The MC56F8300DSK demonstration board is available for \$79 and includes the Metrowerks (www.metrowerks.com) CodeWarrior Development Studio for 56800 with the Processor Expert autocode generator.

—by Robert Cravotta

► **Motorola**, www.motorola.com.

SHARC swims toward deeper, more fertile waters

ANALOG DEVICES' 32-BIT floating-point DSPs have achieved notable success in high-end consumer- and professional-audio applications, as a perusal of the plethora of SHARC logos on ads in publications such as *Electronic Musician*, *Mix*, *Recording*, and *Stereophile* attests. Melody 32, Analog Devices' first stab at mainstream automotive- and home-audio success, netted limited results, due in part to its single-MAC (multiply-accumulate) and fixed-point-only temperaments. The company's ensuing shot, in the form of four simultaneous product announcements, restores SHARC's SIMD (single-instruction multiple-data) and floating-point features to match customers' expectations and competitors' capabilities but converts from a RAM-only internal-memory architecture to a blended RAM-plus-ROM approach to keep costs in line (see "Home theater attracts another DSP supplier," *EDN*, Sept 20, 2001, pg 22).

The 200-MHz, \$14.95 (10,000) ADSP-21266, also available in a 150-MHz, \$12.50 variant, has for six months been available for sampling and will enter volume production in the first quarter of 2004. This nonvolatile-memory-inclusive derivative of the in-production ADSP-21262 includes 2 Mbits of dual-port RAM and 4 Mbits of ROM. The \$9.95 ADSP-21267 variant runs at 150 MHz and has 1 Mbit of SRAM and 3 Mbits of ROM. It is due to become available for sampling in the first quarter. It will house all of the ADSP-21266's ROM-inclusive algorithms *except* for the 24-bit, 96-kHz variant DTS, for which you need to employ either internal RAM or external memory (see "Auditioning high-resolution surround-sound compression," *EDN*, July 10, 2003, pg 89). The ADSP-21267 also offers four serial ports versus six in the ADSP-21266 and 14 "zero-overhead" DMA channels versus 22 in the ADSP-21266.

The \$19.95 ADSP-21365 and \$24.95 ADSP-21364, sched-

uled to begin appearing in sample form in the first and second quarters of 2004, respectively, represent a more extensive revamping of Analog Devices' SHARC architecture. From memory- and processing-performance standpoints, they're identical, both containing 3 Mbits of RAM and 4 Mbits of ROM and running at 300 MHz. The devices achieve the boost in clock speed by moving from the three-stage pipeline of ADSP-2126x products to a five-stage approach. They differ in the mix of audio-tuned peripherals surrounding the DSP and memory cores. The ADSP-21365 integrates an S/PDIF (Sony/Philips digital interface) transmitter-and-receiver combo, DTCP (digital-transmission content protection), AKE (authentication and key exchange) and cipher hardware, and an eight-channel ASRC (asynchronous sample-rate converter) with claimed 110-dB dynamic range.

The ADSP-21364 drops its sibling's S/PDIF and DTCP capabilities but boosts the ASRC SNR specs to 142 dB with input-sample sizes as large as 24 bits, input-sample rates to 192 kHz, and input-to-output sample rate ratios ranging from 7.75-to-1 to 1-to-8. Both chips carry forward the ADSP-21266's six serial ports, boost the number of SPI (serial-peripheral-interface) channels to two and DMA channels to 24, and add 16 PWM channels. All four DSPs are pinout-compatible with each other in the 136-bump BGA package; their flexible signal-to-pin-routing capabilities enhances this feature. The 2126x variants also come in 144-lead LQFPs. They include four-output clock-generation capability deriving from subdivisions of a single input-crystal frequency and support decoding of Microsoft's eight-channel, high-resolution Windows Media Audio Professional format.

—by Brian Dipert

► **Analog Devices**, 1-408-222-2500, www.analog.com.

► **A supercomputer made from 1100 off-the-shelf Apple Macs at Virginia Tech now ranks third among the world's 500 fastest supercomputers, many of which easily handle 1 trillion calculations per second.**

Handheld steps up channel-power-measurement capability

By Graham Prophet

WILLTEK HAS UPGRADED its handheld spectrum analyser with the release of a new software package. The 9101 is a low-cost spectrum analyser

that you can use in applications such as mobile-phone-service centres and wireless-local-loop testing and for 2.4-GHz WiFi systems. You can also use it as a low-cost, compact bench instrument for general-purpose testing. With a frequency range of 100 kHz to 4 GHz, the 9101 can test all commonly used wireless local oscillators and measure harmonics and spurs in the signal band. It weighs less than 5 lbs, including battery, and has a colour VGA LCD

screen with 140° viewing angle. The new software release adds features such as limit templates to allow rapid pass/fail testing to predetermined values or to published standards. Upgraded channel-power measurements allow you to determine radiated power in a specified channel bandwidth, and an AM/FM-demodulation function allows you to monitor signals acoustically using a built-in loudspeaker.

The instrument has a dis-

played average noise level, in a 10-kHz resolution bandwidth (the minimum supported), of better than -105 dB to 3600 MHz. Level accuracy is ± 1 dB, and dynamic range is 65 dB.

► **Willtek**, +49 89 996 410, www.willtek.com.



You can make 4-GHz spectral and channel-power measurements in the field, with three-hour battery life, with the new software upgrade to Willtek's 9101 spectrum analyser.

Communications IP adds SPI interface to FPGA

LATTICE SEMICONDUCTOR has extended its programme of combining high-speed functions for the communications sector with programmable logic with the introduction of its ORSPI4.

As you might infer from the serial number, this chip will handle traffic in the SPI (system-packet interface) 4.2 standard; in fact, there are two SPI 4.2 cores, plus four 3.7-Gbps SERDES blocks, an embedded quad-data-rate memory control, and 16,000 elements of FPGA on the chip. SPI 4.2 is increasingly used as a high-speed parallel interface between processing elements running at line speed.

The “hard” IP occupies about one-quarter of the ORSPI4; programmable logic gates and look-up tables (in the ORCA architecture and supported by Lattice tool sets) take up the rest. Pinout resources mean that if you use the SERDES functions, you can use only one of the SPI cores. The device comes in package options with more than 1000 balls, in either a low-power plastic package or a thermally enhanced package

that dissipates more than 10W, depending on configuration.

Dynamic timing—adjusting the signal-sampling points on a per-pin basis, set up in a “learning” mode—allows maximum data rates of 450 MHz DDR (900 Mbps). Complete built-in calendar logic supports 256 logical ports with on- and off-chip buffering,

and further FIFO interfaces connect to the FPGA array for custom processing. You can select and combine on-chip blocks to perform a range of functions that require SPI; you might use both SPI 4.2 blocks to bring in, process, and bridge traffic to another standard, or you might bring in traffic on one port, perform some manipulation in the FPGA, and send it back out on the other. The part costs \$250 (10,000).

—by Graham Prophet

► **Lattice Semiconductor**,
+44 1932 582941, www.latticesemi.com.



Lattice's ORSPI4.2 adds a further high-speed interface to the company's communications-oriented programmable-logic series.

Upgrade to brushless dc motors with sensorless driver chip

IN AUTOMOTIVE APPLICATIONS, the BLDC (brushless-dc) motor is gaining ground over commonplace brushed types. Brushless motors offer higher reliability—brushes are often the parts that wear

out and promote failure—and they can help you realise greater efficiency. You need lower peak currents to obtain the same mechanical output, and the motor may also be smaller and lighter. However, you need to generate a full three-phase set of waveforms to drive the motor, which is the function of Toshiba's TB-

9060FN motor-controller IC. The 24-pin chip accepts a PWM (pulse-width-modulated) control signal from a host microcontroller and has internal blocks for computing the rotational position of the motor, determining waveform lead angle, and generating the timing for the three output phases. It outputs gate-drive

signals to drive six external power switches, and it includes overcurrent protection and position-detection circuitry that operates directly from the drive waveforms.

As the auxiliary functions on cars become more "electric"—using separate electric motors to perform functions that a mechanical drive from the main power plant previously handled—Toshiba is seeing interest in using BLDC motors to drive cooling water pumps, oil pumps, and in-tank fuel pumps. You can also expect to see them used for secondary functions, such as

washer pumps. In many of these applications, you can upgrade on/off control to continuously variable control, reducing electrical and audible noise. The TF9060FN is rated to 125°C to meet automotive specifications; it operates from 5V, and you can use it with a variety of power-transistor packs to drive a range of motors.

—by Graham Prophet
►Toshiba, +49 211 52960, www.toshiba-europe.com.

Power-over-Ethernet chip uses smart-power technology

FOLLOWING THE RATIFICATION of the IEEE 802.3af standard for PoE (power-over-Ethernet) in recent weeks, PowerDsine has introduced a highly integrated IC to manage PoE distribution in equipment such as multiport hubs. The chip is built in Motorola's (www.motorola.com) SmartMOS8 technology, allowing power switches to be integrated on to the same die as the control logic; the PD64012 is therefore a complete PoE manager for 12 channels, to which you need add only three passive components per channel. For a typical 48-port switch design, the total component count to add PoE is less than 200, PowerDsine says. The chip includes functions such as detection of PoE-service demand, real-time port protection (current-limiting into a fault condition), and ac or dc disconnection. Devices identify themselves according to categories, setting how much power you can expect them to use, and the device sets protection levels accordingly.

You can cascade the chips for designs of more than one port and set a power budget for the complete configuration. Power is typically provisioned statistically, on the basis that not all ports will together be drawing maximum power. One chip in a cluster can act as controller, with the rest of the chips slaved to it, or all chips can cede control to a host-system controller. This provision is necessary if your design needs to detect and provision power to equipment designed before the standard was ratified; otherwise, the embedded standard-compliant software is sufficient. Interchip communication is by I²C bus.

PowerDsine's chief executive officer Igal Rotem anticipates PoE's becoming a dominant standard for the provision of power to both small LAN-connected items of equipment and to small-demand items that may not be using the Ethernet connection. Such equipment would use the PoE connection simply as a matter of convenience. Rotem expects the first design for a mobile-phone-battery charger with an RJ45 plug to emerge very soon. The PD64012 will cost \$18 (1000). —by Graham Prophet

►PowerDsine, +44 208 622 3107, www.powerdsine.com.

FPGAs go flip-chip to serve vertical markets

XILINX HAS DISCLOSED the details of a new architectural design style on which it will base future high-density programmable products, including future members of the Virtex Pro line.

With manufacturers now adding features such as embedded IP, high-speed I/O, and mixed-signal functions to high-end FPGAs, the structure recognises the disparate nature of these circuit blocks and allows for their separate development. Xilinx will marry appropriate groupings of circuit blocks—FPGAs plus others, as required—to provide “platform” chips specific to given application areas. Geometrically, Xilinx says it will base the ASMBL (application-specific modular-block architecture) on columns, or “stripes.” A generic signal-processing platform might, for example, bundle together FPGA, memory, embedded or “hard” DSP

cores, and, perhaps, high-speed I/O in separate columns. Separate teams at Xilinx would develop, verify each function, and shape it into a “stripe” to fit the new architecture. The company says that the ASMBL structure will allow it to rapidly bring the groups together.

Xilinx simplifies interconnect within the chip by the use of leading-edge processes with 10 or more layers of metal. The company simplifies interconnect off the chip by the use of flip-chip technology (as for dense DRAMs), so that you can take I/Os from anywhere on the chip surface and need not bring them out to a chip boundary. Chip archi-

tectures are now free, the company says, to vary the ratio of logic to I/O as required on a given chip design and are not constrained by the perimeter-to-area relationship that comes into play when all I/Os are on the periphery. Likewise, you can now directly feed power and ground to the most power-hungry functions; they need not make their way in from the edge of the chip.

The architecture leaves open the possibility that Xilinx might create a chip that has no programmable logic at all. A company spokesman acknowledges such a chip as a possibility but says it is not a programme objective. The first domain-specific products based on the architecture will appear early next year; 2004 will also see the first product to be built with 10^9 transistors, Xilinx says.

—by Graham Prophet

► **Xilinx**, +44 870 7350 600, www.xilinx.com.

24-bit DAC directly drives audio-power amplifiers

WITH CIRRUS LOGIC'S CS4351 digital-to-analogue converter, you can build an audio-signal chain that Cirrus says will save as much as 20% in bill-of-materials costs over previously available solutions. The company has used a high-voltage process to integrate a number of functions previously discretely implemented; the chip effectively eliminates analogue-signal-processing circuitry for a digital-audio design by providing direct line-out signal drives at a full 2V voltage swing. The integrated amplifier block includes a lowpass filter.

In the digital domain, the stereo DAC is a 24-bit-resolution part running at a 192-kHz sample rate. Dynamic range is quoted at 108 dB, and the corresponding THD+N figure is 95 dB. Outputs are single-ended, and the signal chain also incorporates the “Popguard” function to prevent any unwanted transients from reaching the audio output. The CS4351 will use 3.3V supplies for its digital circuitry and 9 or 12V for its analogue blocks (with separate supplies to reduced coupled noise). Cirrus will package the device in a 20-pin TSSOP.—by Graham Prophet

► **Cirrus Logic**, +44 1491 414030, www.cirrus.com.