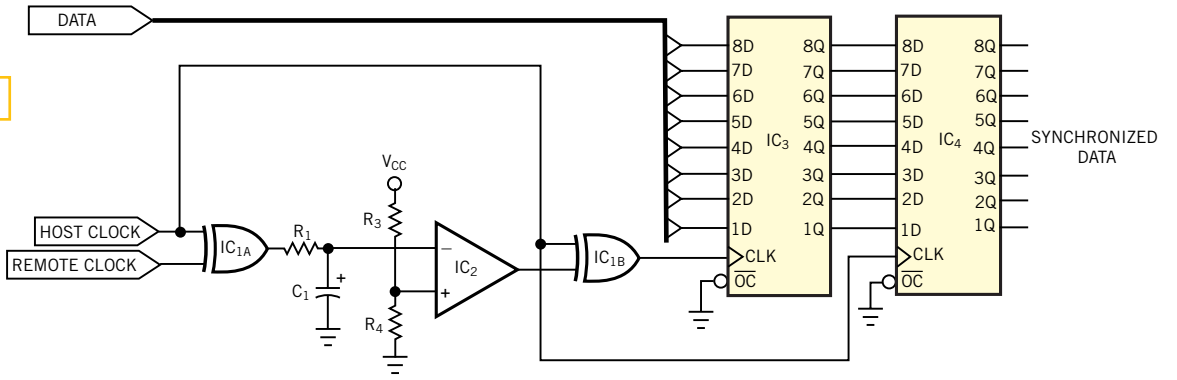


Figure 2



This circuit automatically chooses between the rising and the falling edge on the host clock for clocking in data.