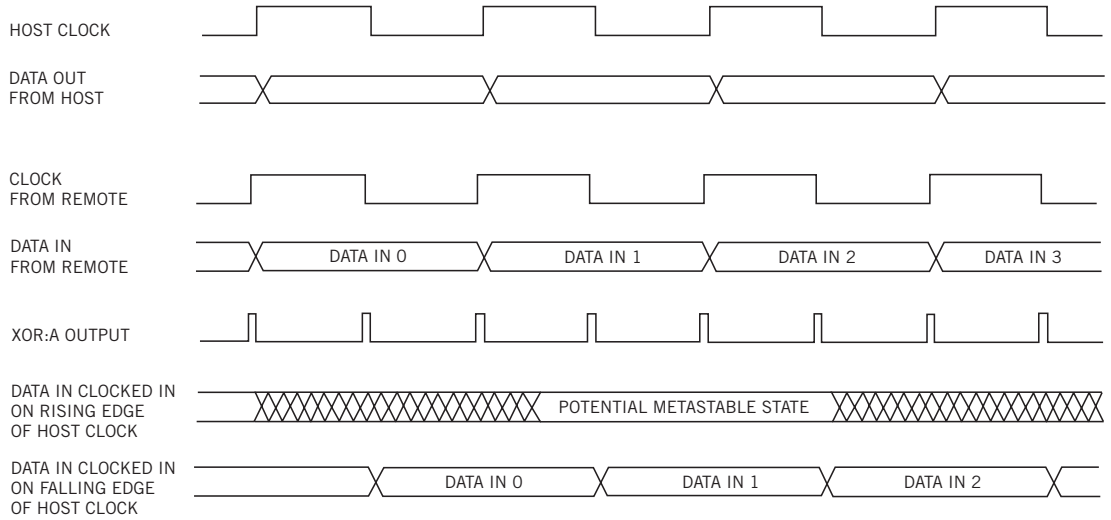


**Figure 3**



**Clocking data on the wrong edge can result in metastability; the circuit in Figure 2 selects the right edge.**