

Palladium from Quickturn packs high computational capability into a small form factor.



# Hardware tools aid engineers in design verification

**HARDWARE ACCELERATION, EMULATION, AND PROTOTYPING: HOW CAN THEY HELP YOU IMPROVE QUALITY AND SHORTEN THE SCHEDULE?**

*At a glance* .....78  
*RTL prototyping: an alternative for real-time system verification* .....78  
*For more information* .....80

**R**ECENTLY, THE DESIGN-VERIFICATION CRISIS has been a hot topic of discussion among engineers. Various research organizations, including Dataquest and Collett International, estimate that design verification requires 50 to 70% of product-development resources. Given that designs are continuously getting larger and more complex, you may conclude that the design-verification problem is new and a direct consequence of SOC (system-on-chip) development. In fact, design verification has been a costly and time-consuming

part of every project for a long time; the problem has become more serious in the last three years. Even before the availability of ASICs, engineers built prototype boards to test their designs and to allow software engineers to develop required codes. These boards took time to build and maintain, which significantly impacted project schedules and budgets. Semiconductor vendors have always spent a significant amount of money developing special-purpose software to aid in the development of each microprocessor and microcontroller. In the '70s, they often developed prototype systems consisting of a number of pc boards to allow the develop-

ment and test of firmware and operating systems. Hardware accelerators designed to speed simulation have been available for almost 20 years, and emulators have been available for more than a decade. The idea of finding a way to accelerate the design-verification cycle is not a consequence of SOC designs. Yet, the higher degree of complexity provides more opportunities for errors; thus, a greater number of cases that need to be checked and the existence of more bugs that need repair complicate the design-verification task.

Hardware accelerators, emulators, and prototyping systems aid designers in functional verification, or front end;

circuit verification, or back end; software and hardware integration; and application-software development.

### ACCELERATORS

Until the middle of 1999, designers used hardware accelerators for both front- and back-end design verification, because gate delays constituted the primary timing elements in a chip. Therefore, a gate model was an accurate representation of the actual device. A traditional hardware accelerator uses synthesis technology to map the RTL description of a circuit into a set of gate-level primitives. You can instantiate the resulting circuit in one or more FPGAs. The accelerator can typically execute the simulation of an RTL netlist 50 to 100 times faster than a software simulator. In a typical environment, an accelerator is connected to a workstation that runs the behavioral testbench and any other behavioral code associated with the design, and the synthesizable netlist of the device under test executes in the accelerator. Because two separate hardware systems execute the system simulation, you need synchronization at every clock cycle, which significantly slows the overall simulation. Therefore, the actual improvement in verification speed is a factor of only four or five.

A more modern accelerator, such as the

#### AT A GLANCE

- ▶ You can use accelerators for front-end simulation and emulators for back-end verification.
- ▶ Products that perform both functions ease the burden for designers.
- ▶ Prototyping can be an efficient methodology for platform-based design.

Hammer from Tharas Systems, uses compiler technology to transform a subset of Verilog into executable code for a sophisticated processor. Hammer uses 128 such processors to achieve a high degree of parallelism. The accelerator is connected to a workstation, but, because Hammer can also execute a subset of the behavioral code, the handshaking between the two boxes occurs considerably less frequently than that which traditional accelerators require. The result is that actual simulation speed can improve by as much as a factor of 50. In the last couple of years, device-fabrication technology has made possible features sizes that are less than 0.2 microns. Interconnect delays now dominate, and gate models can no longer meet the required accuracy for design verification at the back end. Hardware accelerators are still useful

for front-end verification when designers must verify that a large RTL netlist behaves correctly in its intended functional environment.

With the exception of Tharas Systems, which provides only accelerators, companies that also sell emulation or mixed products offer other hardware accelerators. Axis Systems' Xcite accelerator uses compiler technology instead of synthesis. It compiles an RTL netlist into a predefined process that a set of special-purpose microprocessors executes. The advantage of using compiler technology over synthesis is that compilers require much lower turnaround time. When verifying design at the front end, engineers make many changes and try different approaches. If each change required hours of synthesis to produce an accelerator-level netlist, the methodology either would be impractical or would require a number of accelerators to execute parallel verification runs, making the approach too expensive. Quickturn, part of Cadence Design Systems, sells the Cobalt accelerator, which also uses custom processors to achieve fast turnaround and faster execution than earlier synthesis-based products.

### EMULATORS

Emulators map the gate-level netlists of ASICs into FPGAs and provide a wire-

## RTL PROTOTYPING: AN ALTERNATIVE FOR REAL-TIME SYSTEM VERIFICATION

*By Kazunori Goto, Senior Engineering Manager, NEC Electronics*

RTL prototyping is a method of improving system evaluation, which is critical to improving design-turnaround time. Note, however, that RTL prototyping does not replace functional verification; you still need to perform RTL simulation before prototyping. RTL prototyping offers an alternative that can be more efficient and less costly than traditional emulation. Like emulation systems, RTL prototyping involves the use of FPGAs to implement SOC (system-on-chip) logic. By leveraging off-the-shelf chips and bonded-out cores to implement functions in memory devices and processors,

RTL prototyping needs only FPGAs to implement custom logic. This strategy avoids the work of developing emulation models for third-party intellectual-property cores and enables high-speed execution—usually at or close to real time. RTL prototyping allows you to run your system hardware and software at high enough speeds to fully evaluate the system's performance, including subjective characteristics, such as audio or video quality. Early hardware and software codesign is also practical.

NEC's recommended flow uses Synplicity's Certify RTL pro-

totyping environment, which automatically manages the differences between ASIC and FPGA architectures to map a design into an FPGA-based prototyping board. With off-the-shelf chips and bond-outs handling most of the design functions, one of today's large FPGAs can usually contain all of the custom logic. Using a single FPGA dramatically improves the prototype's speed because you avoid the severe I/O delays involved in large FPGA arrays.

To expedite prototype development, NEC offers the Corebest system to its ASIC customers. With one or more

FPGAs, it provides basic system resources, such as a processor, various types of memory, standard peripherals, I/O buses, and interfaces for a logic analyzer and in-circuit emulator. Because you need to mix and match these resources, NEC separated them into three types of boards. A motherboard furnishes an Ethernet interface and several types of I/O-bus connectors. A CPU board and as many as seven intellectual-property boards plug into the motherboard. NEC offers intellectual-property boards that incorporate two FPGAs, and you can also use standard PCI boards.

for-wire and gate-for-gate mapping, as well as a direct interface to the rest of the hardware system. Emulators also offer in-circuit-debugging capabilities that allow engineers to run the circuit in real time yet and set breakpoints and single-step the execution one cycle at a time when troubleshooting the design. Because emulators represent the design at the circuit level, designers have always used them to verify the design after synthesis. Designers also use emulators, like accelerators, with workstations that execute testbenches as well as user interfaces for the debugging software. Unlike accelerators that need to synchronize at every clock cycle, emulators need to synchronize only at every transaction. Therefore, an emulator can execute a number of operations at hardware speed before it needs to perform another handshaking operation with the workstation.

Emulator products today are responsible for a significant number of patent lawsuits. Quickturn and Mentor Graphics are involved in probably the longest lasting legal battle in this field, but Ikos and Axis have also sued each other. Aptix is involved in a patent-related legal proceeding as well. Few ways exist to efficiently translate an RTL design into an executable FPGA-based equivalent circuit; thus, actual solutions have a high probability of unintentionally stepping

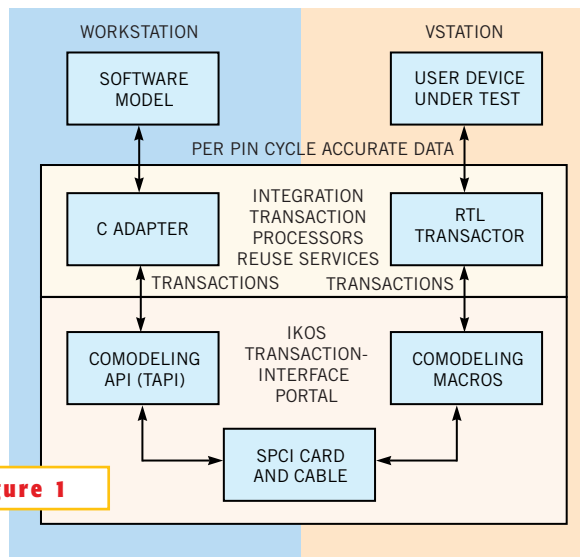
onto some parts of previous patented work. At least the emulation industry is doing its best to provide gainful employment to members of the legal profession.

The advent of commercial virtual components has opened a new verification market that Aptix Corp is serving with its System Explorer emulation prod-

sis state. You can simultaneously emulate a number of virtual components and thus support efficient system-level debugging and verification. The eSOCVerify service allows companies to take advantage of Aptix hardware and expertise by renting time on System Explorer hardware. Via secure Internet links, customers

submit the design they want to emulate. An Aptix application engineer executes the emulation synthesis and simulation run and returns the results to the customer via the same secure link. Mentor Graphics faces a peculiar situation. Its Celero emulation platform enjoys significant popularity in the rest of the world, but Mentor cannot sell Celero in the United States because of the patent litigation with Quickturn. This year, having received a sympathetic nod from a Portland, OR, judge, Mentor launched its own Internet-based emulation service. Using Celero's systems in France, Mentor allows its customers to upload their designs to its emulation center. Application en-

gineers run both the emulated and the simulated portions of the simulations and return results to the customer via the Internet. In addition to Aptix's System Explorer, US system companies that want to have their own in-house emulator systems can purchase Quickturn's Mercury emulator, which allows designers to ver-



**Figure 1**

**Ikos' Vstation-5M architecture provides acceleration, emulation, and hardware and software integration.**

uct and its Internet-based eSOCVerify verification service. Aptix uses traditional synthesis methodology to translate the RTL netlist of a virtual components into FPGAs primitives that allow you to emulate a part of the design as if you implemented it in hardware while the rest of the system remained in its presynthe-

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ify multimillion-gate, equivalent-ASIC devices, even if they have a number of asynchronous clocks.

Although emulation technology can support the verification of large designs, it uses a database different from that of acceleration, which makes it difficult for a design team to correlate the results of presynthesis, or front-end, simulation using an accelerator with the results of postsynthesis, or back-end, verification using an emulator. EDA vendors have addressed this problem by offering products that are both accelerators and emulators in one box.

### HYBRID PRODUCTS

The fact that engineers have to use two systems—accelerators for front-end simulation and emulators for back-end verification—requires additional training, adds to capital costs, and complicates the correlation of results between the two systems. EDA vendors have acknowledged the problem and are now offering products that you can use as either accelerators or emulators. The other advantage is that the database and the user interface are the same, no matter which function the product performs. These two facts significantly ease the burden on designers and verification engineers. Axis, Ikos, and Quickturn have products that meet this description. All three products use compiler technology to parse the design into behavioral and acceleratable or emulatable code and then compile the emulatable code into a set of primitive operations executable at real-time speed.

Axis Systems' Xtreme product uses reconfigurable-computing technology that provides software simulation, accelerated simulation, system emulation, and hardware and software co-verification. You can use Xtreme with a workstation that provides the user interface and executes the behavioral portion of the design and testbench. In the case of hardware and software co-verification, the workstation also executes the software portion of the device under test. By supporting event-based algorithms for both acceleration and emulation, Xtreme eliminates the need for design modifications, minimizes the risk of simulation mismatches, and simplifies debugging.

Ikos' Vstation-5M is also an accelerator and an emulator in one box (**Figure 1**). Ikos has formalized the synchroniza-

## PLATFORM-BASED DESIGN IS ONE OF THE METHODS YOU CAN USE WITH SOC DESIGNS TO MINIMIZE THEIR COMPLEXITY.

tion functions between the workstation and Vstation-5M into a proposed protocol standard that it calls SCE-API (Standard Co-Emulation Application Programming Interface). Recently, Ikos donated the proposed standard to Accellera ([www.accellera.org](http://www.accellera.org)) with the goal of developing an industry-standard-interface specification between a workstation and an external device that provides acceleration services, emulation services, or both. The benefits of such a standard to users are obvious: You can connect any software simulator or debugging tool executing on any workstation to any hardware accelerator emulator from any vendor, as long as both adhere to the standard.

The latest product offering available in this category is Quickturn's Palladium, housed in a box not much larger than a workstation tower. IBM fabricates Palladium's processors in state-of-the-art, 0.12-micron, seven-layer CMOS technology. The product contains 64 custom chips per board, and each chip contains 256 processors. Each board provides as many as 8 million gates for acceleration or emulation. In consultation with each customer, Ikos determines the exact configuration of each Palladium to optimize the price and performance ratio. Engineers considering the purchase of a Palladium box can expect to pay 33 cents per ASIC gate in their design. To optimize the communication between the workstation and Palladium, Quickturn has independently developed its own transaction-based API. Both Ikos and Quickturn have indicated their willingness to work together through Accellera to develop a transaction-based API standard.

### PROTOTYPING

Platform-based design is one of the methods you can use with SOC designs to minimize their complexity. This methodology starts with a set of known hardware and possibly software in the

form of an RTOS and, in certain cases, device drivers, known as a platforms. Designers add product-specific hardware and software to this system. When designers employ such a methodology, it becomes practical to use a prototyping system for system verification. Synplicity Inc sells Certify, a prototyping product (see sidebar "RTL prototyping: an alternative for real-time system verification") that automatically maps an ASIC netlist into its FPGA equivalent. Aptix has a similar capability, Design Pilot, to help designers map the circuit into System Explorer.

Cynergy System Design provides OSP (Open Simulation Platform), which allows virtual-component vendors to offer an encrypted C model for system integration. You can then connect it to the platform and use it in place of the actual hardware for evaluation and early verification. Other providers of integration platforms are CardTools, whose NitroVP product helps in the co-development and verification of hardware and software systems, and SimPod Inc, whose DeskPod II allows a software simulator to interface via a PCI bus with a silicon chip. Simutech also provides the Rave Prototyper System and eValab Internet service, which uses Rave boards to allow both virtual-component evaluation and system prototyping. One of its emulation centers is located in Scotland at the Alba Centre whose Institute for System Level Integration provides skilled support and ongoing research in this area.

Systems designers and integrators have a variety of tools available for system-simulation and -verification. The choice depends on the phase of the development, the complexity of the design, and the price of the tool. □

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