

**THE ACPI SPECIFICATION IS A PLATFORM-INDEPENDENT, INDUSTRY-STANDARD APPROACH TO OS-BASED POWER MANAGEMENT. ACPI ALLOWS INEXPENSIVE POWER-MANAGEMENT HARDWARE TO SUPPORT VERY ELABORATE POWER-STATE TRANSITIONS, MAXIMIZING THE COMPUTER'S POWER CONSUMPTION AND RESOURCE-UTILIZATION EFFICIENCIES.**

# The ACPI advantage for powering future-generation computers

TODAY'S COMPUTERS REPRESENT a quantum leap in performance and complexity compared with the technology available only a few years ago. Nevertheless, a paramount goal of these late and future designs is to make this complexity transparent to users. With minimal setup and intervention, these computers will be able to wake up to perform routine maintenance, download software updates, send and receive fax transmissions, answer the telephone, download audio and video streams, and, when the tasks are complete, go back to a low-power sleep state in which they consume less power than a night light. This type of operation is available in the world of IAPCs (instantly available PCs).

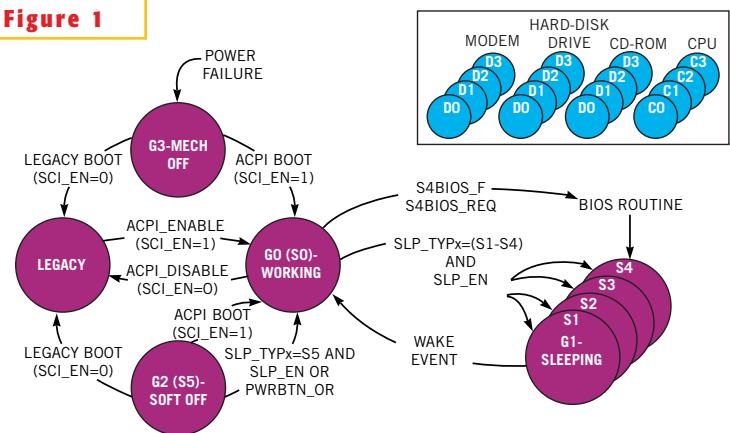
Picture the following scenario in an office setting. A computer system powers up in the morning, and the CPU and all other system components receive regulated power from the onboard dc/dc regulators that operate off the ac/dc supply, also known as the "silver box." During the day, the user may leave the computer unattended for coffee breaks or meetings. Upon a predetermined lack of user input, the computer transitions into a stand-by (sleep) mode during which it consumes minimal power while still monitoring all input ports for incoming data. Depending on the stand-by mode, the PC responds to inputs, such as an incoming fax through the PCI slot or a keystroke, by resuming normal operation in a timely manner. IAPC systems may be able to modify their performance by clock throttling and changing the CPU core voltage on the fly to match user and application demands. These and other advanced modes of operation enable the computer systems to consume energy in the most efficient manner while providing an enhanced user experience.

A number of factors limit the function and flexibility of many of the computer systems in use today and ultimately deprive them of becoming truly intelligent machines. For example, the information

available to the BIOS restricts the implementation of power-management algorithms. Other limiting factors are the lack of a well-specified power-management and configuration mechanism to address advanced system architectures, such as Universal Plug and Play, and the existence of legacy hardware, such as the ISA slots and serial and parallel ports.

The ACPI (Advanced Configuration and Power Interface) specification provides a platform-independent, industry-standard approach to operating-system-based power management. The ACPI specification is the key constituent in OSPM (Operating System Directed Power Management). OSPM and ACPI apply to all classes of computers, including handheld, notebook, desktop, and server machines. In ACPI-enabled systems, the BIOS, hardware, and power architecture must use a standard approach that enables the operating system to manage the entire system in all operational situations. The ACPI OS takes over the power-management and Plug and

**Figure 1**



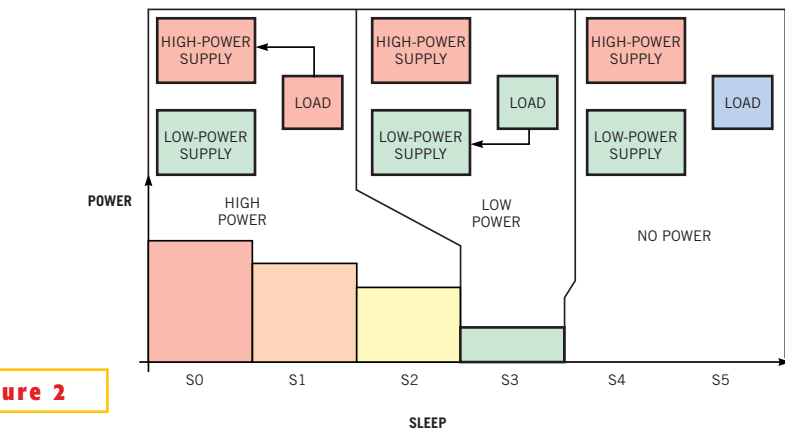
**The ACPI specification defines six discrete operating states—S0 to S5—in order of highest to lowest power consumption.**

Play functions from the legacy BIOS interfaces and allows inexpensive power-management hardware to support elaborate power-state transitions, maximizing the computer's power consumption and resource-utilization efficiencies.

The ACPI OS can put the whole computer or parts of it in and out of various sleep states, based on user settings and application requests. This OS has prior knowledge of how docking or undocking, device insertion and removal, or thermal events affect specific devices. The OS calculates the battery's remaining capacity and life and determines the various battery warning levels in mobile PCs. The OS allows other drivers within the system to communicate and use the resources of system embedded controllers.

**HARDWARE-IMPLEMENTATION CHALLENGES**

From a computer-power-system designer's viewpoint, ACPI power management means generating and managing a



**Figure 2**

**A dedicated power supply for each group of active and sleep states maximizes power-delivery efficiency.**

multitude of voltages on the motherboard and riser cards with no user intervention, to enable the processing of audio, video, and data streams. ACPI-compliant computers require the generation of these multiple voltages at various current ratings as the system transitions

between sleep states. The ACPI specification defines six possible discrete system operating states, which are referred to as S0 to S5, in order of highest to lower power consumption (Figure 1).

All states correspond to some level of power management. In the S0 state, the

**ACPI POWER CONTROLLERS**

The HIP6501A was the industry's first integrated device targeting the ACPI (Advanced Configuration and Power Interface) power-management initiative. The HIP6501A regulates and controls three voltage planes (Figure A). The output voltages are fixed, eliminating the need for external resistors. The HIP6501A interfaces with the computer system

through four digital lines, which allows you to configure the IC for four support configurations, as well as for using a South Bridge IC to control the HIP6501A. The HIP6501A uses only eight external components and operates from a six-pin narrow-body SOIC package.

The HIP6501A integrates three linear controllers: a 5VDUAL for a

USB, a keyboard, or a mouse; a 3.3VDUAL for a PCI, an auxiliary, or a LAN; and a selectable 2.5V/3.3VMEM for systems with RDRAM (Rambus-DRAM), SDRAM (synchronous-DRAM), or DDR SDRAM (double-data-rate synchronous-DRAM) memory. The IC also provides adjustable soft start, internal compensation, overtemperature and undervoltage protection with centralized fault reporting.

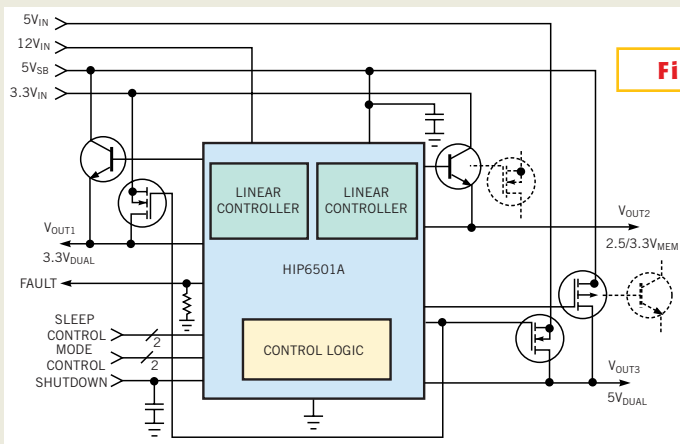
The IC has built-in filters for noise immunity and requires no glue logic.

The small-pin-count package and the small number of external components do not impede on the chip's functions or ease of use. Wherever possible, the chip was designed to be compatible with bipolar transistors, reducing system cost over implementations using MOSFETs. Thus, a bipolar pnp transistor

can replace the PMOS switch employed on the 5VDUAL output. For systems employing RDRAM or DDR SDRAM memory, the HIP6501A uses a bipolar npn as a pass element of the corresponding output. For SDRAM-based systems, an NMOS transistor replaces the npn pass element. An HIP6501A-based ACPI circuit typically eliminates a minimum of 29 external components compared with a fully discrete ACPI power-management implementation.

Other ICs, such as the HIP6500B, HIP6502B, and HIP6503, can regulate and control five voltage planes, including 3.3V standby and 2.5V clock supplies. The HIP6500B and HIP6502B typically eliminate a minimum of 35 external components of a fully discrete ACPI power-management implementation.

The HIP6500B, HIP6501A, HIP6502B, and HIP6503 use an ATX ac/dc supply ("silver box") and work with the HIP6020/21 and ISL6523/24 four-in-one PWM controllers to simplify the power-supply design on ACPI-compliant motherboards.



**Figure A**

**The linear controllers of the HIP6501A provide 5VDUAL for a USB, a keyboard, or a mouse; a 3.3VDUAL for a PCI, an auxiliary, or a LAN; and a selectable 2.5V/3.3VMEM for systems with Rambus-DRAM, synchronous-DRAM, or double-data-rate synchronous-DRAM memory.**

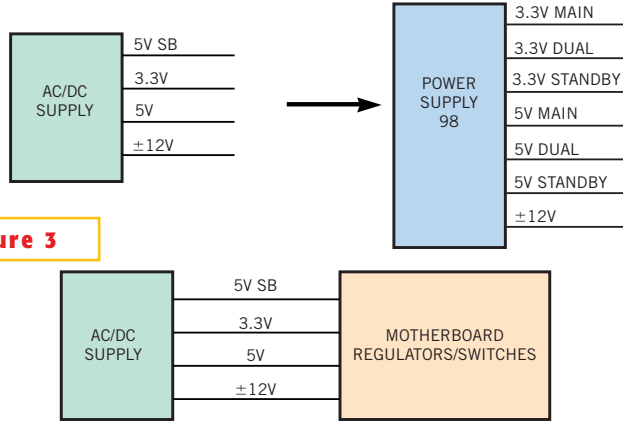
CPU may toggle between C0 and C1 or C2 states, and the power system must be able to quickly respond to resultant current transients. Other system components have their own corresponding power states, D0 to D3, which best match their usage profile based on user and application needs. As the system transitions into lower power states, the power consumption decreases.

The lowest power consumption comes in the sleep states of S3 through S4, in which the computer system slips into a virtual shutdown. A typical system will supply standby power to system memory, USB and PS/2 ports, and LAN card or modem circuitry in an S3 state. The same system will typically remove standby power to the system memory and modem when entering an S4 state and will remove power to all components except the power button when entering an S5 state.

The deep, power-saving sleep states come with drawbacks. The more circuitry that shuts down to conserve energy, the longer it takes to restore the system to an operational status. Power-management challenges arise when these systems transition between these various states. A system in an S3 state that wants to go into an S4 state must first go to an S0 state, perform the required tasks, then enter the lower power S4 state. The onboard power-conversion and power-management circuitry must generate and enable the appropriate voltage and current levels as the system makes a glitch-free transition into the various states. Hardware-design and -implementation quality is important, because a power anomaly at any transition point could cause severe problems, including loss of user data.

**THE “DUAL”-POWER-SUPPLY CONCEPT**

Intel introduced the concept of the “dual supply” in the Power Supply 98 initiative, which discusses how to deal with the power-supply demands of computer subsystems during their operation in various states. A supply powering a computer subsystem in an ACPI environment must be able to supply the full active current yet drop into a low-power mode when the subsystem itself slips into a



**Figure 3**

**Implementing dual supplies on the motherboard allows for application flexibility and custom configurations.**

low-power sleep state. To maximize power-delivery efficiency, it makes sense to have a dedicated power supply for each group of active and sleep states. Thus, this concept leads to a high- and a low-power supply and to matching the power needs of the subsystem with the appropriate power supply (Figure 2).

The system can implement the dual supplies either within the ac/dc power supply itself or directly on the computer motherboard. However, traditional ac/dc supplies are not user-configurable. Thus, if computer manufacturers want to use a dual-mode silver box, they must pay for the cost of full ACPI support in every purchased power supply, regardless of whether the computer or the motherboard is capable of handling it.

Implementing the dual supplies on the motherboard allows for application flexibility and custom configurations, as well as cost advantages if the project calls for limited support of ACPI features (Figure 3). In this implementation model, a series of onboard regulators and switches is necessary to generate these voltages and to switch between supply rails as the subsystems change operating modes.

**DISCRETE VERSUS INTEGRATED APPROACH**

A fully discrete implementation may initially seem to be the simplest and most cost-effective method of regulating the various ACPI power states and the transitions between them. You can realize the various onboard regulators for system memory, PCI slots, USB, keyboard, and mouse using voltage references, resistors, capacitors, op amps, diodes, and bipolar and MOS transistors. Such discrete implementations have many drawbacks, the most important of which are the subject

of many technical articles. Noise coupled into the circuits leads to “illegal” ACPI state transitions and power perturbations that can lead to loss of critical data. Switching between supplies while they have not fully stabilized or switching several loads into the same supply line leads to power overloads, which can cause momentary brownouts, leading to output regulation falling outside design limits. Interfacing the various discrete regulators to the South Bridge IC requires additional glue logic that is not immune to system noise. Glitches may trick

the regulators into entering a fault state or latch off.

You can realize good discrete implementations, but typically, a discrete ACPI power-management circuit takes up precious board area and lacks system-monitoring and -protection functions that could reduce the total cost of ownership and prolong the life of an ACPI-compliant computer. The surface-mount-placement cost associated with these discrete components also contributes to a higher implementation cost. Additionally, the potential reliability of the computer is less than that of an integrated option, because there are many more components on the board that could fail.

ICs that combine the ACPI regulators and system-monitoring and -protection functions necessary to manage the operating-state transitions and the power demanded are an economical, simple, and reliable method of ACPI-compliant-motherboard power management (see sidebar “ACPI power controllers”). □

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