

WITH PORTABLE APPLICATIONS ON THE RISE, DESIGNERS ARE TURNING TO DYNAMIC POWER-CONSERVATION TECHNIQUES TO DELAY THE INEVITABLE DEAD BATTERY.

Dynamic voltage scaling conserves portable power

REDUCING POWER CONSUMPTION in portable equipment continues to drive innovation across all areas of IC design and will continue to do so well past the day when systems can operate solely on the power that body heat generates. Whether or not you believe this statement, one thing is certain: IC suppliers are on constant alert to reduce power wherever possible.

DSP and microprocessor suppliers for portable applications pay extraordinary attention to integrating power-saving capabilities wherever possible. However, once their processors have been selected for applications and “designed in,” it’s up to systems engineers to actually squeeze more power out of the processor and surrounding system. One way to accomplish this goal is by using specific power-supply ICs and a technique called DVS (dynamic voltage scaling). This technique is attractive for portable, battery-powered systems, in which low power is critical to prolonging operating time. Most portable applications—such as PDAs, Internet audio, MP3-players, and digital still cameras—do not require the DSP’s full processing power

all the time, creating an opportunity for power conservation. The key to a successful design, however, is selecting the components that allow for DVS.

RUNTIME CONTROL

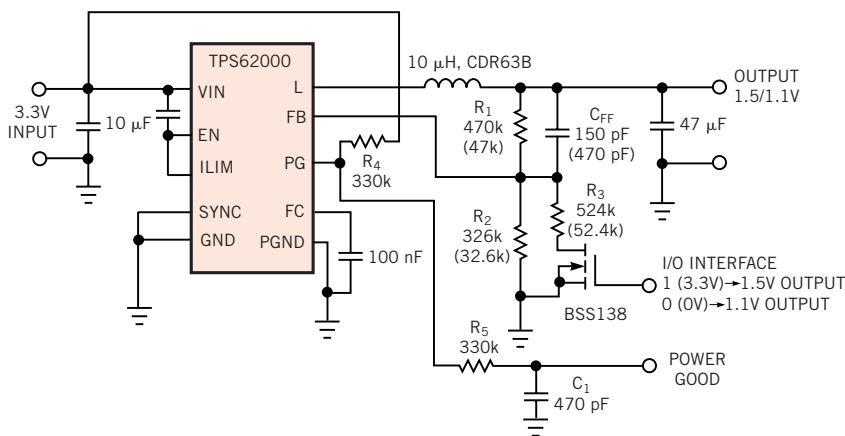
When you don’t need maximum performance from a DSP or microprocessor, you can lower its core supply voltage, and it can operate at a reduced clock frequency. The DVS technique, or runtime power control, adjusts the supply voltage to the required core performance. The technique itself is a matter of programming the DSP to send a signal to a DVS-capable step-down or buck converter, usually via a GPIO (gen-

eral-purpose-I/O) pin. Future-generation low-power applications will most likely implement this technique, or something similar, to maximize system-power conservation. In actual measurements of an MP3-player application using a DSP and a TMS62000 buck converter, implementing DVS resulted in a 23% reduction of the DSP’s overall core power consumption (**Reference 1**). The bottom line: DVS extends battery life in handheld applications.

The power supply for most DSPs in portable applications usually comprises an I/O supply and a core supply. A 3.3V supply typically powers the I/O peripherals within the system; the core supply provides a voltage of less than 2V and powers only the data processing within the DSP. Of particular importance to DVS is the minimum supply voltage of the core. It depends on the required clock rate, which is a function of the DSP performance for the given application at a given time.

Using the aforementioned MP3-player applica-

Figure 1



A typical DVS (dynamic-voltage-scaling) circuit uses an off-the-shelf dc/dc converter to generate the adjustable supply voltage.

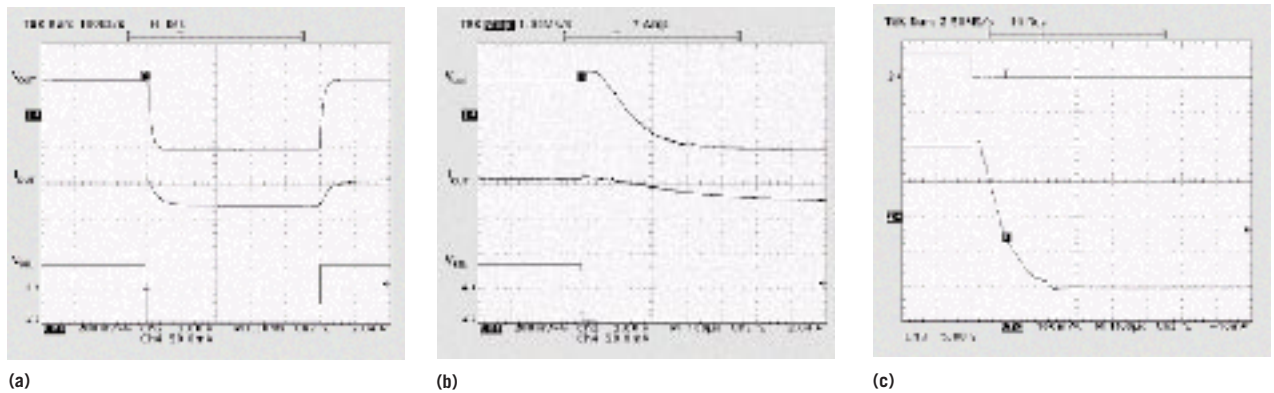


Figure 2

A complete voltage-scaling cycle varies the output voltage between a low of 1.1V and a high of 1.5V (a). When switching V_{SEL} from a high to a low level, the gate-drain capacitance of the MOSFET causes a small voltage overshoot on V_{OUT} (b). The V_{OUT} overshoot reduces to less than 20 mV with lower values for the feedback-resistor network (c).

tion, you can implement DVS by switching the core supply between 1.5 and 1.1V. $PC \sim (V_C)^2 \cdot F$ describes the power consumption of a DSP core, where PC is core power consumption, V_C is core voltage, and F is the core clock frequency. As shown, lowering the internal clock frequency can reduce the power consumption; lowering the core supply voltage can reduce it even further.

You can best understand DVS by examining the circuitry surrounding an MP3 application that uses DVS with a DSP engine and is powered by a commercial buck converter. For most portable applications, you should use a high-efficiency buck converter that is designed for battery applications, possesses ample current, provides very high efficiency, and supports DVS. Decreasing core supply voltages in modern DSP systems and the need for better efficiency make using a synchronous

step-down converter more efficient than using a low-dropout regulator.

DVS CIRCUIT

Figure 1 illustrates a circuit used to implement DVS. The 3.3V system supply powers the TMS62000 buck converter. You use an input signal from one of the DSP's GPIO pins to select the requested core voltage. Variation of the feedback-resistor network ad-

justs the core voltage from 1.1 to 1.5V. The MOSFET modifies the resistive voltage divider connected between the output of the dc/dc converter and its feedback pin (FB) by inserting another parallel resistor. This application uses a general-purpose BSS138 MOSFET with V_{GSTH} of 1.6V. The GPIO 3.3V port drives the MOSFET. The feedback-resistor network consists of R_1 , R_2 , and R_3 . C_{FF} is a feedforward capacitor that the compensation network of the regulator uses for improved regulation.

The best way to modify the resistor network is by switching R_3 in parallel with R_2 . In doing so, you ensure that the parasitic capacitance of the MOSFET has the least influence on the regulation behavior of the dc/dc converter. The proposed MOSFET has an $R_{DS(ON)}$ of less than 10 Ω . This value is small compared with the values of the resistive divider

and is, therefore, negligible in the calculation of the resistance values of the modified resistive divider.

The general requirements for this application are:

- output voltage 1 (DSP core)=1.5V;
- output voltage 2 (DSP core)=1.1V;
- input voltage=3.3V; and
- output current=150 mA (with a 10 Ω load).

To keep the current and power losses through the adjustment resistor network as low as possible, the resistors are set to $R_1=470$ k Ω and $R_2=326$ k Ω .

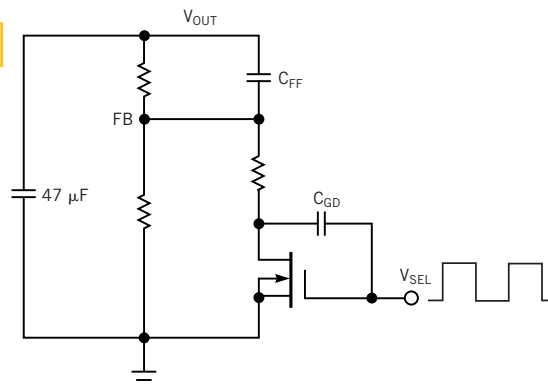
Because $R_2 \parallel R_3=201$ k Ω , R_3 is set to 524 k Ω . This resistor choice means the quiescent current through the resistor network is less than 2 mA. This value is about 4% of the typical 50-mA quiescent current of the converter. A 150-pF capacitor for C_{FF} reduces the influence of the MOSFET's gate-drain capacity during switching.

Figure 2a shows a complete voltage-scaling cycle. I_{OUT} is the output current, powered in a 10 Ω load. V_{SEL} represents the I/O voltage applied to the MOSFET gate. A low level of V_{SEL} scales the output voltage to 1.1V; a high level scales it to 1.5V.

MOSFET INFLUENCE

In Figure 2b, switching V_{SEL} from a high level to a low level generates a small voltage overshoot on V_{OUT} . The gate-drain capacitance of the

Figure 3



You can reduce the influence of the gate-drain capacitor, C_{GD} , by increasing the value of the feedback capacitor, C_{FF} .

MOSFET, which injects the negative edge of V_{SEL} signal into the feedback-resistor network, causes this overshoot.

You can reduce the influence of the gate-drain capacitance by using lower values for the feedback-resistor network. Lower resistor values result in higher values for C_{FF} . If you change the resistor values and lower them by a factor of 10 to $R_1=47\text{ k}\Omega$, $R_2=32.6\text{ k}\Omega$, and $R_3=52.4\text{ k}\Omega$, C_{FF} increases to 470 pF. With this modification, when

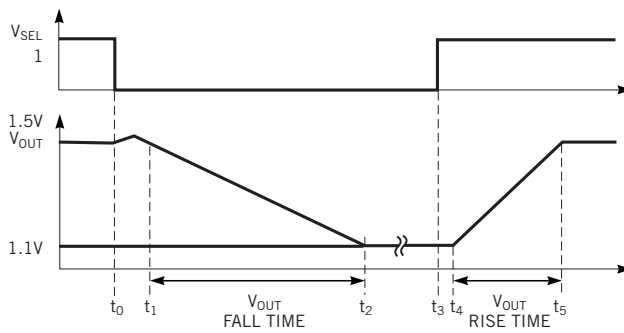


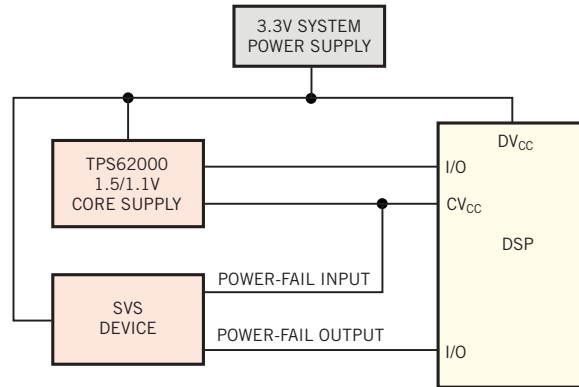
Figure 4

During the fall time of V_{OUT} , the load must absorb the energy stored in the output capacitor until the lower voltage is in regulation.

you switch the converter to regulate to 1.1V, the overshoot decreases to less than 20 mV (Figure 2c).

Figure 5

Figure 3 shows the feedback-resistor network and the MOSFET-effective capacitor, C_{GD} . If you increase the value of C_{FF} , you reduce the influence of the gate-drain capacitor, C_{GD} . Therefore, C_{FF} works as a low-impedance connection to V_{OUT} and minimizes the docked V_{SEL} signal at the FB pin. You can further reduce the influence by using a MOSFET with a lower internal capacitance (instead of a general-purpose MOSFET).



An SVS (supply-voltage-supervisor) circuit monitors voltage amplitude to detect core-voltage power failures.

TIMING CONSIDERATIONS

The timing behavior of V_{OUT} depends heavily on the values you use for the output and input capacitors, coils, and feedback-resistor network. This situation is especially true for the fall time of V_{OUT} , which depends on the output current as well as the inductor and output capacitor. During the fall time, the load must absorb the energy stored in the output capacitor until the lower voltage is in regulation.

In Figure 1, the power-good comparator has an open drain output, which becomes active-high if the output voltage exceeds 94.5% of its nominal value. The dynamic variation of the resistor

network can affect the power-good-detection circuit, because it compares the FB voltage with an internal reference. Depending on the output current, a short power-good spike can occur during the rise time from a 1.1V core level to 1.5V. Use an RC filter on the power-good output to eliminate this short spike and to obtain a defined power-good signal. R_4 is the power-good pull-up resistor, and R_5 and C_1 form the RC-filter network.

After the core voltage reaches 1.5V, you can again switch the DSP to higher internal clock rates. To do so, you must detect the time, t_5 , when the dc/dc converter output is in regulation (Figure 4). You can achieve this goal by either of the following alternatives. You can activate a software timer after the DSP initiates the

control signal to increase the supply voltage. Because the rise time of V_{OUT} is application-specific, the designer must determine it based on measurements. You can generate a CVD (core-voltage-detect) signal by using the power-fail comparator of an SVS (supply-voltage-supervisor) circuit having an internal 1.25V reference. This method detects the exact moment at which the 1.5V core voltage fails. As many processors request negative edges for interrupt generation, inverting the CVD signal can be useful. The 3.3V system supply supplies the SVS circuit. External resistors can adjust the threshold voltage for core-voltage detection. Figure 5 shows the basic block diagram of this circuit.

DVS is a simple approach to reducing core power consumption of next-generation DSPs and microprocessors. It requires only a high-efficiency step-down converter, a few additional passive components, and a general-purpose MOSFET, and, where power consumption is critical, the benefits of reducing the core power consumption more than compensate for the few additional components. □

REFERENCE

1. TPS62000 datasheet from Texas Instruments, <http://www.ti.com/sc/pdsheets/slvs294a/slvs294a.pdf>.

AUTHOR'S BIOGRAPHY

Bill Chew is a strategic marketing manager at Texas Instruments' Semiconductor Division, where he has worked for 14 years developing strategies for, assisting in the new product definition of, and promoting state-of-the-art power-management ICs. He has worked on low-dropout regulators, dc/dc converters, supervisory circuits, and many other products. He has a BSIE from Louisiana Tech University (Ruston) and enjoys golf and softball.