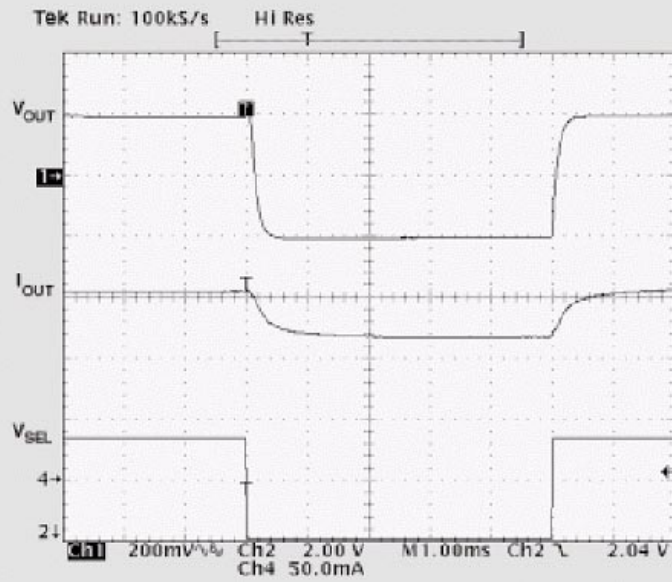
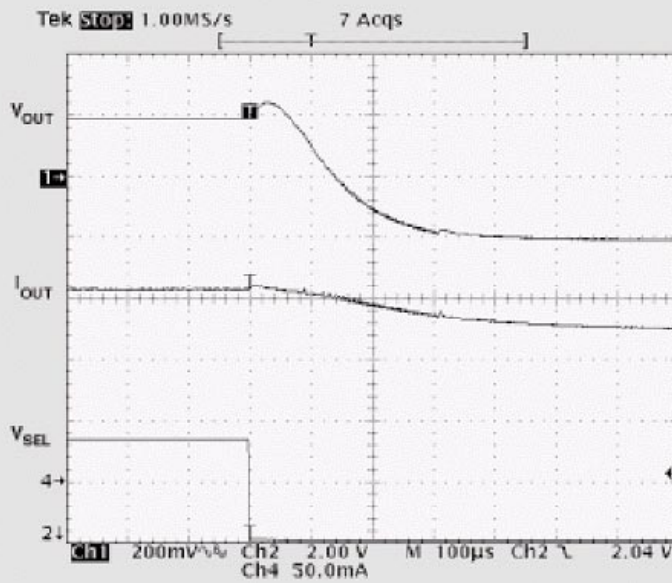


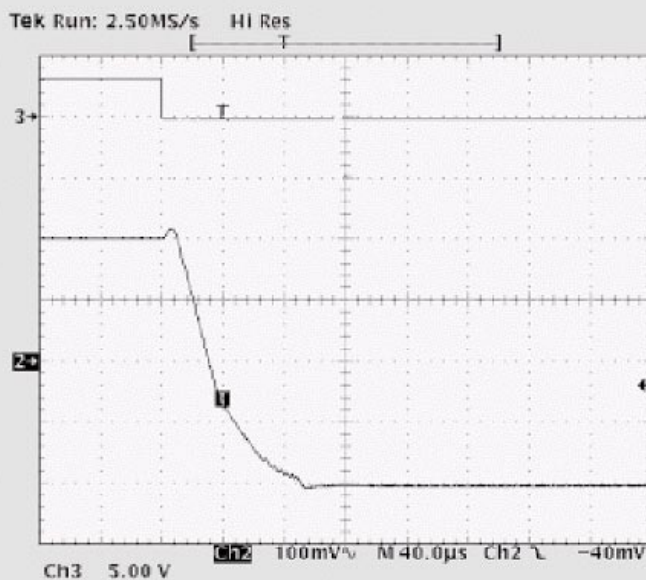
Figure 2



(a)



(b)



(c)

A complete voltage-scaling cycle varies the output voltage between a low of 1.1V and a high of 1.5V (a). When switching V_{SEL} from a high to a low level, the gate-drain capacitance of the MOSFET causes a small voltage overshoot on V_{OUT} (b). The V_{OUT} overshoot reduces to less than 20 mV with lower values for the feedback-resistor network (c).